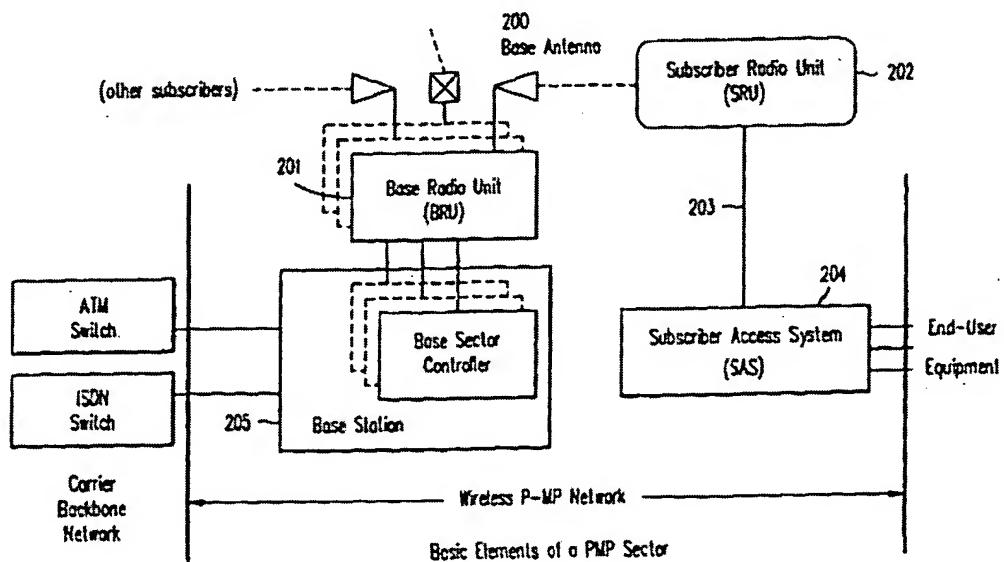




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(54) Title: WIRELESS ATM METROPOLITAN AREA NETWORK



(57) Abstract

The present invention provides an efficient point-to-multipoint microwave ATM network including a base station (BS 205) broadcasting a continuous transmission with a sector antenna (200). The system uses time division multiplex (TDM) for downstream transmission and time division multiple access (TDMA) for upstream transmission. The downstream transmission consists of ATM cells encapsulated in MAC protocol data units (PDUs) for forward error correction (FEC) and synchronization. Small Subscriber Terminals (STs), including Subscriber Radio Units (SRUs 202), receive the broadcast and pass it to a Subscriber Access System (SAS 204) that drops the ATM cells addressed only to them. To allow strong FEC protection and to maintain the same symbol rate as the downstream transmission without sacrificing bandwidth, a modified trellis code modulation technique, which incorporates Reed Solomon coding, is used during upstream transmission.

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WIRELESS ATM METROPOLITAN AREA NETWORK

5 Field of the Invention

This invention relates to the field of telecommunication networks and packet switching and, in particular, to providing radio-based point-to-multipoint for cell-switched networks.

10 Background

The Asynchronous Transfer Mode (ATM) method of transmitting and switching multimedia information is replacing older circuit and packet switching techniques, allowing flexible, fast and cost effective provision of new telecommunications service. Among these services are Internet access, Basic rate ISDN, fractional T1/E1 support of cellular PCN network and LAN traffic routing.

15 These services require expensive infrastructure of transmission facilities, such as copper lines, fiber optics, cable TV or hybrid fiber-coax (HFC). In a competitive environment in which some new telecommunication service providers own some or none of the above facilities, wireless is the other alternative for timely and cost effective deployment of transmission networks. Two previous patent applications (Application Serial No. 08/388,110 filed February 13, 1995 and Application Serial No. 08/538,327 filed October 3, 1995 both assigned to the same assignee and both incorporated herein by reference in their entirety) disclose the structure of reliable networks based on point-to-point radio links. These links allow 20 reliable transmission of ATM traffic with minimum link errors and ATM cell misinsertion. These links are cost effective for applications with high bandwidth and continuous transmission. However, these systems make bad use of equipment and spectrum for applications of intermittent nature such as telephone calls over a wireless link. When a telephone is on hook, the spectrum should be freed for other 25 potential users, and so should the central office transceiver that served that

telephone. Data traffic does not always follow the behavior of voice calls. Data may flow slowly, requiring low baud rate for transmission, followed suddenly by a burst of high speed traffic. For efficient use of spectrum, it is desired to allocate bandwidth on demand in a fast and efficient way to handle such bursty
5 information.

These requirements can be served by a multiple access network that uses ATM cells to emulate the variety of services, and by the use of a media access control (MAC) protocol to arbitrate the transfer of data over the air.

10 ATM services include Constant Bit Rate (CBR), suitable for telephony and video, Variable Bit Rate (VBR), suitable for video applications with variable compression, Available Bit Rate (ABR) suitable for data transactions, and Unspecified Bit Rate (UBR), suitable for e-mail or other non-delay sensitive applications. A MAC layer must support efficiently all of these services.

15 Due to the high bandwidth required for serving many customers with varying bit rate requirements, high total bandwidth is required in such links. This bandwidth is available only at high microwave frequencies, usually in the range of 10-40 GHz.

20 The economy of point-to-multipoint systems favors delegating as many functions as possible to the base station ("point") serving the subscriber terminals ("multi-point"), thus saving the cost of replicating the same function in all terminals.

25 There is, therefore, a need for a point-to-multipoint wireless metropolitan area network with MAC layer suitable for a variety of ATM services, operating at microwave frequencies and allowing cost-effective subscriber radio terminals.

25

Summary of the Invention

30 This invention provides an efficient point-to-multipoint microwave ATM network (sometimes called a "system"). A base station (BS) broadcasts a continuous transmission with a sector antenna. The system uses time division multiplex (TDM) for downstream transmission (from base to subscribers) and time

division multiple access (TDMA) for upstream transmission. Existing TDMA protocols, such as those used in HFC applications, use a periodic frame with time slot numbers to indicate who can transmit. This technique is suitable for telephony applications where each voice call occupies a fixed bandwidth, i.e. a fixed number of slots. This technique suffers a major drawback when used in ATM applications. Some ATM CBR rates have periods which are different from other CBR services, that are non suitable for a TDM frame. With different periods, there may be no common frame period to fit all. Eventually, either ATM cells will have to be dropped when their timings coincide, or the ATM network will not admit connections with such conflicts, resulting in low bandwidth utilization. In accordance with this invention, ATM cell transmissions in the upstream direction are granted on a cell by cell basis. If two upstream cells coincide, one is shifted slightly in time, causing small cell delay variation (CDV) which is preferable to losing that cell. The downstream transmission consists of ATM cells encapsulated in MAC protocol data units (PDUs) and other overhead bits used for forward error correction (FEC) and synchronization. Small Subscriber Terminals (STs), including Subscriber Radio Units (SRUs), receive that broadcast and pass it to a Subscriber Access System (SAS) that drops the ATM cells addressed only to them. Each MAC PDU transmitted by the BS may include a grant for a specific ST. The grant specifies which ST is allowed to transmit but not which time slot. The time slot of transmission is implicit in that the time slot is simply a fixed number of time slots from the grant reception event.

The upstream transmission includes single ATM cells with their MAC and physical layer overhead. To allow strong FEC protection and to maintain the same symbol rate as the downstream transmission without sacrificing bandwidth, a modified trellis code modulation technique is used. Trellis code modulation includes transmission of redundant code bits for error correction. In accordance with this invention, the trellis code rate is increased, causing it to weaken its noise immunity, i.e. more bits are excluded from the trellis code overhead. For example, the code rate is increased to 5/6 from 2/3, meaning 5 out of 6 bits are data and only

one out of 6 is trellis code overhead. However this weakening is more than compensated for by using the extra bits for Reed Solomon coding. The combined concatenated code has better noise immunity than a TCM code alone (at a lower code rate), yet they both use the same symbol rate and the same payload.

5 The Subscriber Radio Units (SRUs) are simplified in design by having them phase locked to the Base Station carrier. In accordance with this invention, the transmit signal frequency is phase locked with a frequency offset to the original signal, thus the phase noise remains almost as low as that to the expensive base station microwave synthesizer.

10 To provide high antenna gain and low cost, an integral lens-horn antenna is used in the SRU. The base station uses a horn antenna that in accordance with this invention includes adjustable beam width by use of absorption plates and an extended main radiation lobe in the vertical dimension by use of a lens or a geometry with intentional phase plane deviation.

15 The ATM traffic gathered from the STs is optionally shaped by a cell jitter attenuator to reduce cell delay variation (CDV) occurring over the link.

16 The Base Sector Controller (BSC) includes the master MAC controller and application-specific processing circuits and software. In the case of supporting basic rate ISDN services, the BSC includes an interworking function that converts 20 individual circuits-emulation ATM cells from each ST to a combined emulated T1 or E1 line with embedded signaling according to V5.1 or V5.2 protocols. This signal can then be combined with similar signals from other BSCs, if desired by an external ATM switch. The combined signals travel via the ATM backbone network until they reach a site with an ISDN central office switch. The signals are 25 then transferred by the ATM switch at that site to a physical T1/E1 line that can be connected to the ISDN switch or other equipment.

This invention will be more fully understood in conjunction with the following detailed description taken together with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a wireless point-to-multipoint (P-MP) network of a type suitable for use in a city.

5 Figure 2 shows the basic building blocks of a P-MP cell site.

Figure 3 shows an example of frequency division of the spectrum for transmission in a sector.

10 Figure 4 shows a cross section of a Subscriber Radio Unit with a built-in lens-horn antenna and with a waveguide extension option for external antenna connection.

Figure 5 shows a block diagram of the subscriber terminal with a focus on frequency control.

Figure 6 shows a block diagram of the digital section of a subscriber access system for a basic rate ISDN application.

15 Figure 7 shows a modem trellis code modulation encoder for the upstream transmission.

Figure 8 is a phasor diagram showing a constellation of 8-PSK modulation.

Figure 9 is a modem TCM trellis diagram with rate 5/6.

20 Figure 10 shows a reference model for the air interface MAC protocol and other protocol layers.

Figure 11 shows a downstream ds.block MAC primitive.

Figure 12 shows another embodiment of the ds.block primitive with a floating payload structure.

Figure 13 shows the upstream primitive us.atm_cell structure.

25 Figure 14 shows the timing relationship between the downstream and upstream slot and pointers relationship as viewed from the base station.

Figure 15 shows the timing concept of bitmap reservation.

Figure 16 shows the admission request primitive.

30 Figure 17 shows the structure of each downstream slot associated with the CellMAC overhead structure.

Figure 18 shows the upstream primitive MAC overhead structure.

Figure 19 shows the concept of MAC SAPs.

Figure 20 shows the handshake between the MAC layer at the subscriber side and the ATM layer.

5 Figure 21 shows ATM cell transmission originating from the ATM layer at the subscriber terminal if bitmap reservation is available.

Figure 22 shows the same transmission as in Figure 21 but with contention reservation.

10 Figure 23 shows the transfer of ATM cells by an ST which is capable of transmitting in four channels.

Figure 24 shows a block diagram of a base station. Figure 25 shows a block diagram of the MAC layer controller at the base station.

Figure 26 shows a block diagram of a base station controller.

15 Figure 27 shows a model of interference from remote base station to a subscriber.

Figure 28 shows the vertical radiation pattern of an unsuitable antenna.

Figure 29 shows a suitable base station antenna.

Figure 30 shows a cellular coverage map with asymmetrical sectors but one pair of frequencies.

20 Figure 31 shows a cellular map with three frequencies.

Definition of Acronyms

Note: Netro-specific terms use ***BOLD ITALIC*** characters.

AAL ATM Adaptation Layer

25 ABR Available Bit Rate, an ATM service in which the source rate may change during a connection wherein cell delay variation is not specified.

AGC Automatic Gain Control

ARM Adaptive Radio-Resource Management

30 ARQ Automatic Retransmit Request

	ATM	Asynchronous Transfer Mode
	BPSK	Bipolar Phase Shift Key
	<i>BRU</i>	Base Station Radio Unit
	BS	Base Station
5	<i>BSC</i>	Base Station Sector Controller
	CBR	Constant Bit Rate - an ATM service with guaranteed rate of transport and cell delay variation.
	CDV	Cell (ATM) Delay Variation
	DC	Direct Current
10	DRO	Dielectric Resonant Oscillator
	DVB	Digital Video Broadcast
	E1	European digital line interface at 2.048 Mbps.
	E2	European digital line interface at 8.448 Mbps.
	E3	European digital line interface at 34.368 Mbps.
15	EPROM	Erasable Programmable Read-Only Memory
	EEPROM	Electrically-Erasable Programmable Read-Only Memory
	FDD	Frequency Division Duplex
	FPGA	Field Programmable Gate Array
	FEC	Forward Error Correction
20	HEC	Header Error Control
	HFC	Hybrid Fiber Coax
	ID	Identification
	IP	Internet Protocol
	ISDN	Integrated Services Digital Network
25	LAN	Local Area Network
	LED	Light Emitting Diode
	LNA	Low Noise Amplifier
	MAC	Media Access Control
	Mbps	Mega bits per second
30	MMIC	Monolithic Microwave Integrated Circuit

	NMS	Network Management System
	P-MP	Point to multipoint
	PBX	Private Branch Exchange, a generic term for a voice switch.
	PCN	Personal Communication Networks - A mobile telephone service
5		type.
	PCS	Personal Communication Services - A mobile telephone service.
	PDU	Protocol Data Unit - the payload field of a protocol packet.
	PN	Pseudo Noise
	PSK	Phase Shift Keying
10	PROM	Programmable Read-Only Memory
	PTT	Post Telephone and Telegraph, a common name for government service providers
	QPSK	Quadrature Phase Shift Keying
	RISC	Reduced Instruction Set Computer
15	RS	Reed Solomon (a block error correction code)
	<i>RU</i>	Radio Unit
	SAP	Service Access Point
	SAPI	Service Access Point Identifier
	SAS	Subscriber Access System - the indoor portion of a subscriber terminal
20	<i>SRU</i>	Subscriber Radio Unit
	<i>ST</i>	Subscriber Terminal (<i>SRU</i> + <i>SAS</i>)
	<i>STI</i>	Subscriber Terminal Identifier
	STM	Synchronous Transfer Mode
25	TBD	To be defined (later)
	TCM	Trellis Code Modulation - an error correction method based on encoding the transition of modulation symbols.
	TDD	Time Division Duplex - transmission and reception at same frequency alternating in time
30	TDM	Time Division Multiplex

TDMA	Time Division Multiplex Access
Terminal	A system consisting of SAS, SRU and the interconnections.
UBR	Unspecified Bit Rate - an ATM service with no guaranteed rate, cell loss ratio or delay.
5 VBR	Variable Bit Rate - an ATM service.
VC	Virtual Circuit. In ATM cells is made of VPI/VCI.
VPI/VCI	Virtual Path Identifier/Virtual Channel Identifier - an ATM address.
XOR	Exclusive OR

10 Detailed Description

A sector of a P-MP wireless transmission is shown in Figure 1. A base station antenna 100 transmits to a sector 101 of 30 to 90 degrees. Subscribers wishing to get telecommunications services have subscriber terminals (STs) installed in their houses or offices. Nearby subscribers may install small outdoor 15 radio units (SRUs)102. Those living far may install a parabolic antenna 103 attached to an SRU. A typical range of a metropolitan area network of this kind is 5 km. The angle of each sector is between 15 to 360 degrees.

The main building blocks of a P-MP network are shown in Figure 2. Each sector antenna 200 is connected to a Base-Station Radio Unit (BRU) 201 that 20 transmits and receives the radio frequency signals. The subscribers have Subscriber Radio Units (SRU) 202, connected by a coaxial cable 203 to a Subscriber Access System (SAS) 204 located typically indoors and attached to the user's equipment such as a telephone, computer, ATM switch or a micro-cellular telephone base station. The Base Station includes Base Sector Controllers (BSC), 25 one per sector. The base station mediates between the service provider's backbone network, i.e. ATM network or ISDN network, and the subscribers terminals.

Each sector's spectral allocation may consist of multiple channels as depicted in Figure 3. For example, a base station carrier may transmit at 25 GHz, occupying 28 MHz of channel width. However, the channel may be further 30 divided into four 7 MHz sub channels so that low-cost STs will not have to

transmit and receive at high speeds. The transmit-receive arrangement in this embodiment is based on frequency division duplex (FDD). For example, the base may transmit at 25 GHz and receive from the STs at 26 GHz. Other sectors may reverse role, having the BS transmit at 26 GHz. Each of the sub channels in turn is 5 divided in the time domain. The downstream transmission is a time division multiplex (TDM) channel, essentially a broadcast to all STs tuned to this frequency, while the upstream transmission is a time division multiple access (TDMA), having the STs transmit in turn, as permission is granted from the BSC.

The SRU, shown in Figure 4, is a small enclosure, roughly a shoe box size 10 400 with a built-in lens horn antenna. The horn 401 is conical or pyramidal. A dielectric lens 402 provides phase correction. The electronics is mounted on a motherboard 403 with various modules 404 attached. A coaxial connector 405 allows cable connection to the SAS. The horn 401 is fed directly from a diplexer 406 or via a coax/waveguide connection. If a larger antenna is desired, the SRU 15 can be mounted in front of a parabolic reflector with the horn antenna serving as a feed; alternatively a waveguide adapter 407 may be installed to allow direct connection to a larger antenna. Mounting hardware similar to a flood light lamp pointing mechanism is used for alignment towards the base station antenna.

To reduce costs, the SRU does not have a microwave frequency 20 synthesizer. Instead, it relies on the stable BRU frequency as a reference. As shown in Figure 5, a free running DRO oscillator provides a rough microwave reference. By using dual conversion, a low frequency synthesizer 501 can create the desired offset frequency and fine tune the reception frequency. Examples of oscillator frequencies are shown in Figure 5. A frequency multiplexer 502, 503 is 25 used for combining all signals onto a single coaxial cable for convenient SAS to SRU connection. The modem recovers a precise carrier of 70 MHz that tracks the phase noise drift of the receive signal, caused mostly by the DRO 500, and uses this frequency for transmission. As shown by formulas at selected nodes of Figure 5, the final transmitting frequency is independent of the DRO; therefore it cancels 30 its phase noise. Another embodiment of this invention includes only one

conversion, i.e. mixers 505, 506 are 507 are eliminated. Although the phase noise cancellation feature is lost in this case, the benefit is fewer spurious signals, the by-products of mixing and hence less filtering demands.

The SRU structure is application dependent. In many applications, only the 5 digital section 508 changes as the applications change. An example of a digital section to be used for a limited number of ISDN basic rate interfaces is shown in Figure 6. A microprocessor 600 with built-in ATM formatting capabilities is used for signaling and controlling the entire terminal. The ISDN interface is provided by off the shelf integrated circuit 601. An ATM access layer for converting the 10 payload to ATM cells can be implemented using a field programmable gate array (FPLA) 602. For an ISDN payload, a method known as AAL1 is suitable. A media access control (MAC) device 603, transmits the ATM cells to the modem section 504, shown in Figure 5. A Forward Error Correction Device 604 and an encryption/decryption device can also be used. The MAC device can be 15 implemented with a gate array. If cell buffering exceeds device capacity, external memory devices (not shown in the drawings) may be added.

Modem 504 operates differently from upstream transmission as compared to downstream. Upstream transmission entails sending bursts of ATM cells while downstream transmission is continuous. Assuming 4-PSK (QPSK) modulation 20 issued in the downstream direction, it is desired to maintain the same symbol rate in the upstream direction. However, to achieve good error control, the short upstream bursts (approximately 64 bytes comprising an ATM cell and its overhead) should be heavily protected, which means large forward error correction overhead, resulting in a reduction of upstream payload throughput. This dilemma 25 is sometimes alleviated by use of trellis code modulation (TCM). In TCM, a higher modulation format is used, for example 8-PSK instead of 4-PSK. Some of the extra bits in the 8-PSK modulator are carefully assigned a linear convolutional code based on the length of the intervals between successive symbol transmissions ("phasor"). These distances are slower in Figure 8. For example, the squared 30 distance between phasors 0 and 4 is 4 (relative to the radius squared). This

technique has some code gain, but is not as effective as Reed Solomon or other similar block codes. In accordance with this invention, the TCM process is modified. First, the code is punctured, i.e. some of the code bits are replaced by data bits. The resulting higher bit rate in turn is used for Reed Solomon (RS) 5 encoding. The overall concatenated code (punctured TCM + RS) has a better code gain than TCM alone for the bit error range of interest to ATM, i.e. a bit error ratio better than 10^{-9} . The modem encoder is shown in Figure 7. A converter 700 converts user serial bits to symbols of two or three bits with the pattern 3-3-2-2-3-3-2-2 $\frac{1}{4}$ bits per symbol. A state machine 701 consisting of one-symbol delay 10 elements and XOR gates 703a and 703b, performs convolutional coding of bit Y1 during a 2-bit symbol transmission. During a 3-bit transmission the state machine switches to the down position of switches 702a, 702b and 702c. The resulting state trellis diagram is shown for the first four symbols in Figure 9. Each branch represents a symbol transmission. Multiple numbers on the same branch represent 15 parallel alternatives of the same state transition. This diagram has a free distance of 2 or more between any two paths that start at the same node and meet at another node. This distance is similar to QPSK, thus the trellis code will perform roughly like QPSK. So far, one half of the extra 50% bits of the modulation gain from 4-PSK to 8-PSK have been used for TCM. The overall code gain is improved by 20 reusing the other half of the extra 50% bits available, that in a 64-byte transmission, allow 14 RS check bytes for error detection and correction plus a few extra bytes for overhead. The modem counterpart in the Base Station receives this encoded message and decodes the transmission using the well known Viterbi algorithm. Even better code performance suitable for this invention is a use of 25 multidimensional trellis code modulation in which groups of symbols, such as two symbols, are aggregated for each step of the trellis code, keeping the code rate at 5/6. In more general terms, a constellation with M bits per symbol is encoded at a rate higher than $(M-1)/M$, which is 2/3 for 8-PSK as in some modulation schemes proposed for cable modems.

An alternative to TCM is to use 4-PSK with a symbol rate increased by roughly 10-30%, and using the extra bits as RS check bytes. The advantage of this alternative is a more robust modulation scheme and the avoidance of a complex TCM trellis decoder.

5 The Base Station demodulator receiving this transmission performs synchronization and decoding. If multipath reflections exist in the propagation path, an adaptive equalizer can be used. Due to the short cell size in ATM transmission, it is not practical to include a long training preamble, thus the equalization is done by means of a multi pass process. First the received signals
10 known as I and Q signals are digitally encoded by A/D converters. The digital samples are then stored and equalizer parameters are estimated. Then the equalizer steps back to the beginning of the message and equalizes using with the estimated parameters. Once this operation is completed, the signals are decoded and demodulated using the Viterbi decoding mentioned above. The equalizer
15 parameters can be stored for next reception from the same source, depending on their time variation.

A reference model for the MAC and related protocol layers is shown in Figure 10: Starting from the bottom, a physical medium dependent layer 1010 provides for the radio transmission and modem functions. The MAC layer 1020 (dubbed here "CellMAC") includes FEC (as discussed above), scrambling and framing 1030. Scrambling is done to randomize the transmission. Framing will be discussed below. The main MAC access attributes are Synchronization 1040 - timing adjustment of the delay to the base station. Encryption 1050 of the ATM cell payload is provided by off-the-shelf DES devices, and public key distribution
20 procedures. Three methods of bandwidth request exist: Contention reservation 1060, Bitmap reservation 1070 and implied reservation. Each of these will be described below. The only type of upstream data transmission is via granted cell transfer 1080, i.e. no cell is transferred without a grant (unique permission) from the base station. A data link control 1090 ("CellDLC") layer is provided for
25 optional cell retransmission. This layer is bypassed in most applications, because
30

good error control and detection is already provided by the physical layer as discussed above.

The ATM layer 1005 maintains queues of cells of different service classes. A separate control queue maintains management-type messages between the base 5 and the STs. Upper layers are similar to any ATM application.

The MAC primitives and rules are now discussed. It should be clear that although the MAC layer is described by abstract primitives, each primitive corresponds to a hardware function suitable for implementation by means of a digital gate array. In fact, the first primitive to discuss, ds.block 1110 shown in 10 Figure 11, is a typical FEC block code ("ds" stands for downstream). Each slot 1101 represents an ATM cell 1102 with its MAC overhead 1100. The block is ended by 16 FEC bytes 1120 of RS code. A slight modification is shown in Figure 12, in which the slots are "floating" relative to the block timing. This arrangement allows decoupling of the slot size from block size so that mass market low cost 15 DVB-standard FEC decoders developed for satellite television receivers can be used. This standard uses 1 sync byte 1200 and 187 payload bytes, forcing the 59- byte slots 1210 to be randomly truncated, where the missing portion is transmitted in the next block. The slot timing recovery is still possible by a process known as 20 ATM cell delineation, based on the fixed position of the cell header error control (HEC) octet (not shown in the drawings).

The upstream primitive us.atm_cell consists of only one cell because each slot may be used by another ST. As shown in Figure 13, the upstream primitive ATM cell consists of 1 octet gap 1300, 4 octet preamble 1310, which uses the 8- 25 PSK modulator as a pseudo random sequence of phasors "0" and "4" (essentially BPSK) to allow the demodulator to synchronize the timing and phase of the incoming signal. The block also includes the MAC overhead 1320, ATM cell 1330, RS check bytes 1340 and a tail 1350 for TCM decoder state resolution.

The MAC layer maintains a fixed timing relationship between each downstream slot and each upstream slot. This allows it to refer acknowledgments 30 of past transmissions and grants of future transmissions without need to specify the

time acknowledged. A fixed system parameter of upstream delay N_{up} and downstream delay N_{down} , all referred to The Base Station timing, is used, RS shown in Figure 14. For example, $N_{up} = 20$ slots offset and $N_{down} = 25$ slots offset. All STs adjust their delay to appear in sync at the base.

5 Bandwidth reservation is done by means of one of three options. Constant bit rate services receive grants periodically without request. The Base Station management program provisions such grants and configures the BSC MAC device to issue periodic grants. In the resulting upstream transmission, the MAC overhead reports the queue status. As a result, the downstream MAC controller can consider
10 this queue status report in prioritizing grants. A second method of requesting a grant is the unsolicited transmission of a short block, us.request, including 1 gap octet, 4 preamble octets, 2 address octets, 2 queue status octets, 2 CRC (error check) octets and 4 FEC (RS) octets. About 5 or 6 of those primitives can fit in one slot time, thus the slot is divided into 5 or 6 "minislots", increasing the
15 opportunities to request bandwidth. From time to time the base station issues global grants indicating a contention slot that allows transmission of these requests. A contention algorithm is used to resolve collisions. This is done by a stabilized slotted aloha or START-3 protocol well known in the literature. For example, an ST maintains a timer that is cleared after every cell it transmits (with queue status
20 indicating more cells waiting). If the timer expires, the ST selects a minislot at random and performs the START3 protocol from the same minislot position in future transmissions. Upon receiving a grant, the ST stops contending until the next timer expiration.

The third method to request bandwidth is the bit map option. Each ST of a
25 limited group (say 110), is provisioned with a single symbol position in a special upstream slot granted as "bitmap" type, as shown in Figure 15. Each ST of the group with expired timers transmits a signal that is equivalent to asserting one symbol. This method is collision free and thus is very fast and efficient. Since it is not practical to detect a single bit transmission, the bit primitive is actually a short
30 PN sequence, for example 15 symbols long. The receiving modem correlates the

received signal by this sequence and records the peaks as individual symbol positions. Although the bitmap sequences overlap, the correlation peaks happen at single symbol times and thus are separable.

The us.admit primitive is shown in Figure 16. This primitive is sent only if a slot is granted as admission slot. Admission is a process of adjusting ST timing and power before the ST is allowed to receive grants for ATM cell (us.atm_cell) transmissions. There are two types of admission messages, cold and warm. A cold admission is a first time request sent by a newly placed ST. The us.admit includes an 8-octet preamble 1600, carrying a PN sequence or a fraction of a PN sequence of 32 symbols using only the phasors "0" and "4". A Subscriber Terminal Identifier (STI) 1601 is then transmitted. A cold ST uses a special temporary STI value of 0001401. A 6-byte IEEE address 1602, similar an to Ethernet address, installed during manufacturing, uniquely define the ST. A 2 octet cyclic redundancy code (CRC) 1603, a 4-octet RS FEC check 1604, and a 2-octet tail 1605 are used. The Base Station Controller grants several consecutive slots for admission requests. These grants are repeated several times per second. The number of slots (say 4) is such that the delay uncertainty of a new ST will not cause it to step on other slots. If the us.admit primitive is received without error, a downstream message will be broadcast to all STs with STI of 0001401 and a management service access point identifier to be discussed in conjunction with Figure 17. This message will repeat the IEEE address and will also include a new STI assignment, a delay figure and a power adjustment figure. If admission failed, a collision indication is placed and the ST must try again in the next granted admission slot group. A START-3 or slotted aloha protocol may be also used to accomplish this function.

A warm admission is used for an ST that already has an STI, but lost sync for some reason. If a warm admission is not successful, a cold admission must be restarted.

The content of a downstream MAC overhead is shown in Figure 17. The first two octets 1700 represent mostly response to the events that took place Nup

slot-periods ago. There are four types of slots: ATM, admission (grouped to four slots), contention(divided to six minislots) and bitmap. All of these slot types have been defined above by the primitive types they carry. The response includes specific bit meaning based on the slot type. The response includes 3 frame bits

5 1710 used for global synchronization of frame (say every 126) slots (the first bit is toggled, else it is zero, the second bit is eight times slower and the third bit is still eight times slower then the second). These bits allow coordination of events, such as starting of a new connection ahead of time, and among many STs. Next are timing adjust 1720 and power adjust 1730 bits. These bits are valid only if the

10 response is to an ATM slot type. The next octet is a response vector. For an ATM slot this next octet acknowledges reception (0) or error (1). For a contention slot this octet indicates collision so that a certain number of bits in this octet correspond to a minislot and the rest of the bits are undefined. For admission this octet represents collision in any of the four admission slots, and this octet value will be

15 repeated for all contiguous admission slots.

The next 2 octets 1770 include STI 1740 and service access point identifier 1750 (SAPI) which is a MAC sub address to be further discussed in conjunction with Figure 19. These fields indicate the destination ST address of the current downstream ATM cell. Some STI values are reserved as group addresses,

20 allowing multipoint broadcast. The ST MAC controller may include several STI registers so that address decoding is ORed with all registers for inputting a cell from the ds.block primitive. The last two octets 1760 are grants for an upstream slot Ndown ahead. The grant includes slot type 1780 (2 bits required, 2 more reserved bits) and STI 1790. The STI is meaningful only if the slot type is ATM.

25 A more formal definition of the above fields is shown in Table 1.

Table 1.

ds.CellMAC	{	
3-BIT	FRAME	/* frame timing
30		/* next 3 nibbles are related
		/* to the upstream inf.

```

      /* sent Nup slots ago
 2-BIT   TIMING_ADJUST /* fine tune ST clock delay
 2-BIT   POWER_ADJUST /* adjust ST transmit power
 BYTE    RESPONSE   /* contention COLLISION vector
 5
      /* (one bit per minislot) or
      /* COLLISION for us.atm_slot

-----
      /* the next two octets are
      /* related to the ATM cell
 10
      /* attached to this.CellMAC

 12-BIT   PAYLOAD_STI /* ST identifier (address)
 NIBBLE   SAPI      /* ST sub-address

-----
 15
      /* the next 2 octets are related
      /* to an upstream slot Ndown
      /* slot from the current one.
      NIBBLE   TYPE      /* slot type, either one of:
 20
      /* us.atm_slot.
      /* contention slot.
      /* bitmap slot
      /* admission slot
 12-BIT   GRANT_STI /* STI for us.atm_slot
 25
      }

```

The upstream MAC overhead is depicted in Figure 18. It includes the STI/SAP of the sender 1800, 12-bit buffer status 1810 and a four bit time stamp 1820. The buffer status is an indication of all ATM cells waiting for transmission in this ST. If none exists, an all zero status is transmitted. Otherwise a map function is defined to map each queue status to this short message. An example of a map is: each four bits represent one of three service priority levels. For each level, the four bits indicate the level of queues utilization, i.e. 0000 is empty, 0001 is 1/16th full and 1111 is 15/16 full or completely full. The queue capacity can be transmitted once by upper management layers, as it is not varying in time. The

time stamp indicates the cell delay variation (CDV) relative to its ideal transmission time in units of slots. If an ST expects a grant for a time sensitive signal at slot x, but receives the grant at slot x + t for a maximum value of T, then t is transmitted as the time stamp. This time stamp allows the BSC to reduce CDV 5 by delaying all cells by T-t slots.

The concept of service access points SAP is shown in Figure 19. ATM SAP 1900 carries user's data while a management SAP 1900 carries BS to ST management information. SAPs 1910 and 1920 are reserved for future use. One potential use is separate a SAP for each ATM service category, such as constant bit 10 rate (CBR), variable bit rate (VBR), available bit rate (ABR) and unspecified bit rate (UBR).

In supporting all of these services, a separate SAP identified by a SAP Identifier (SAPI) allows direct connection to each type of queue, e.g. the MAC circuit has one port per SAP. The implementation of the queues is application 15 specific. Queue-control hardware and software are widely available from ATM switch components and LAN interfaces vendors.

The operation of the MAC layer can be described by ladder diagrams. Figure 20 shows a simple handshake of the ST MAC layer 2000 commanding the ATM layer 2010 to send a cell. The ATM layer 2010 returns a pointer 2020 to the 20 data (cell) in memory and the queue status. The cm.send primitive 2030 can be implemented by a signal on a specified pin in a MAC gate array, and the data/status can be implemented by buses on the same IC. A convenient way to implement the data bus itself is the Utopia Bus as defined by the ATM Forum. The handshake of Figure 20 implies that a send command comes from the MAC, 25 rather than being initiated by the ATM layer. Therefore, the ATM layer will transmit only when a grant is received. However the ATM layer can indirectly request transfer, as shown in Figures 21- 22. Figure 21 shows an atm.have_data primitive (again, just an interface pin or an electric signal), initiating transfer by requesting bandwidth via the bitmap mechanism combined with status. The MAC 30 2110 sets the appropriate bit (i.e. it sends the bitmap PN sequence) when the

downstream indicates a grant type bitmap. Then the bitmap is set (us.have_data 2120 represents setting the bit) and eventually a grant arrives, enabling the transfer. Figure 22 illustrates similar schemes, but without a bitmap, which employs contention via a minislot. The bitmap is faster and therefore preferred; however if 5 it is not implemented, the contention mechanism of Figure 22 is used.

So far the MAC protocol has been described for a symmetrical single channel transmission with frequency duplexing, such as a single 7 MHz channel. However this protocol can be extended with minor changes to fit other situations. One such occurrence is when the downstream signals run N times faster than the 10 upstream signals. Each set of STs receives the fast signals but responds on one of N separate channels. In this arrangement, the slots are simply multiplexed in the downstream in the sequence: SLOT1_CHAN1, SLOT1_CHAN2, SLOT1_CHAN3, SLOT2_CHAN1, where the STs can identify their stream of slots by observing the change in the frame bits as discussed in 15 conjunction with Figure 17. The first frame bit to toggle corresponds to channel 1. Another extension is an ST that needs to transmit on all four channels. This may happen in some higher capacity applications. As shown in Figure 23, for N=4, the N channels are skewed in time so that channel i starts 1/N of a slot time after channel i-1. As a result interleaved cells arrive in the order in which they were 20 transmitted. Figure 23 shows cells transmitted from a single ST in the order 1,2, 3,4 skipping busy slots. Each transmission in a slot occurs because of a grant to that ST.

Although the MAC protocol as described is a frequency division duplex (FDD) structure, it can also be applied to time division duplex (TDD) with slight 25 modifications. The main modification is that the correspondence of downstream slots to upstream slots for purpose of response and grants is defined relative to upstream slots on the same frequency channel. If the upstream and downstream directions have asymmetrical bandwidth allocation, the downstream being N times wider than the upstream, then only one of the N downstream ATM cells carries a

MAC overhead and the other N-1 ATM cells are transmitted without any MAC overhead.

In accordance with this invention, grants are not directed, i.e. when an AT receives a grant to transmit a us.atm_slot primitive, the ST chooses which one of 5 the currently available ATM cells to transmitt. This freedom preserves link bandwidth by avoiding transmission of the cells virtual circuit number (VPI/VCI in ATM terminology). However, a potential problem may arise if a grant intended for constant bit rate (CBR) service arrives too early and is used for an other service (say ABR) only to find out later that there will be no other grant for this ST. This 10 problem is solved by the following algorithm. The BSC maintains a list of all CBR connections and their period and the last slot that was used in the upstream for this connection. The BSC calculates the new expected grant time and the BSC normally grants this slot to the ST with this circuit. However, if due to conflicts of two or more CBR circuits at different rates whose expected slots coincide from 15 time to time, only one of them will be granted and the rest will be delayed within a time window W1 of 10 slots. Each CBR circuit handler at the ST (such as the AAL device 602 in Figure 6) maintains a window of period W2 slots (say W2=10, but needs not be equal to W1) starting with the expected slot. Only grants for slots within this window may be granted to this connection. If multiple connections 20 have overlapping windows, the window that started earliest, i.e. the oldest window will get the grant, as long as it has not expired will get the grant. This process causes cell delay variation anytime the grant is not available for the circuit at the beginning of the window. The CDV can be eliminated using the time stamp mechanism discussed above.

25 The MAC protocol can be implemented in several ways. One approach is to delegate all time critical functions to a field programmable gate array (FPGA) with attached memory devices, encryption/decryption devices and forward error encoding/decoding devices. The FPGA block diagram for a subscriber terminal is shown in Figure 24. The ds.block primitive is decoded externally and the 30 recovered data, clock, error detection and timing signals 2400 are brought to the

FPGA. If needed, the demodulator 2410 is informed specifically of which ST is expected in the current slot time. This enables the demodulator 2410 to store and retrieve the contents of the latest known power level of this ST, thereby reducing the chance of error or the acquisition time of power level and frequency offset.

5 The slot timing is recovered first by a timing and cell delineation circuit 2401, with the aid of a cell header error control checker 2402. Next, the address field STI in the MAC overhead is checked by an address decoder 2403 to check if the currently received cell should be dropped for local use. Several STIs are compared - one is the local STI (which equals 0 if the admission process has not been completed)

10 Several group addresses may also be checked. A dropped cell is delivered to the application via the RxData bus 2404 which may be the Utopia Bus. Next the grant type and grant STI are examined by the address decoder 2403, and if the grant is locally valid, it goes to a grant buffer 2405 and delayed by Ndown slots compensated to the ST's specific distance from the base station by a delay generator 2412, whose specific delay value has been set by an external microcontroller during the admission process. The grant type and timing are signaled to the various upstream primitive generators by a grants bus. This controls the generation of bitmap requests 2406, minislot request 2407 (us.request), us.atm 2408 and us.admit 2409. Each of these primitives is generated

15 by a bit sequence loaded from an external microcontroller except for status and data that are passed directly from the application. The transmitted signal with appropriate timing indications is sent to the modulator 2411 which also performs encoding and scrambling.

20 The Base Station MAC control section is shown in Figure 25. This section may be implemented on a printed circuit board level, including multiple memory and FPGA devices as may be required. The MAC controller receives MAC primitives from the burst demodulator via a bus 2500. This bus indicates data, timing, estimated reception power and error messages. A timing generator 2501 controls the reception and transmission of MAC primitives. It is synchronized via external timing reference means and control signals 2502 allowing the slot timing

to be frequency locked to a global synchronization such as the telephone network primary clock or global positioning system. If the reception slot is an admission slot, the admission parameters are estimated based on the modem input 2515 by an estimation circuit 2502. If admission request is detected, it is passed to the Base 5 Sector Controller via an indication bus 2507. In a us.request reception, the minislot processor 2505 decodes the request and deposits the queue status from the request into a register bank called queue table 2508. Similarly, if a bitmap slot is received, all set bits are written into the queue table 2508 by the bitmap processor (decoder) 2506. Other conditions on a reception, such as normal us.atm_cell cell 10 reception and loss of data, are decoded by a Status Reader 2504. The Status is written to the queue table 2508, and the indication of success or failure of reception is indicated to the Response Generator 2503. The response generator updates the response field in the ds.block primitive via a multiplexer 2509. A grants processor 2510 scans the queue table and selects the ST to receive a grant. That ST's address 15 (STI) is written in the address field of the multiplexer 2509. The grants processor 2510 makes its grant decision not only according to the queue content 2508 but also by a connection table 2511 that lists all constant bit rate virtual circuits (VC). Thus, for each such VC it checks whether the next upstream slot to be granted should get a grant related to this VC. Only if none of the CBR VCs has a non- 20 expired window of transmission a grant based on the queuing table 2508 is selected. Once a grant is made, the related STI and SAPI are read from the connection Table 2511 and sent to the multiplexer 2509. The grant processor 2510 can be implemented by a combination of an FPGA and a RISC processor. The FPGA performs a priority encoding (decision) of the next ST, while the RISC 25 processor performs the background tasks of maintaining the queue table. For example, if a particular ST is selected by the Grants Processor 2510, the queue status entry for that ST is modified according to the following algorithm:

1. Modify Queue status for this ST as it would appear after one cell is 30 subtracted from the highest priority queue.

2. If a new status is received from the same ST (via us.request or us.atm_cell), the new status overrides the modified one.
3. If no valid cell was received from the ST at the granted slot (most likely due to link error) and no new status update of step 2 was done, then restore 5 original queue status.

Cells to be transmitted downstream arrive from the application layer which can be an interface circuit to the ATM network. The cells are delivered in the order in which they are received by a cell input circuit 2512, to which the cell 10 destination address (ST and SAPI) is added by an ST Mapper 2513 based on a connection table 2511. There are two ways to implement the STI Mapper, depending on the choice of ATM address space in a particular ATM application. If all STs share the same address space (VPI/VCI), then the Connection Table 2511 assigns an STI/SAPI to each VPI/VCI. In other applications, the address space 15 may have only local context (two STs may reuse the same VPI/VCI of their ATM cells for totally unrelated connections), then the ATM application must provide the STI/SAPI for each cell to be sent. The application in this case is most likely an ATM switch or an ATM statistical multiplexer that can treat each ST as a logically separate port.

20 The multiplexed downstream transmission is handed to the modulator, scrambler and FEC encoder via a transmit bus 2514. If needed, the cell input circuit 2512 may add encryption to the payload field (48 bytes) of the ATM cell.

A base station Controller, shown in block diagram in Figure 26, consists of 25 one or more single channel controllers 2600, and a linear frequency division multiplexer 2601. Each single channel controller 2600 includes an IF circuit 2602 (amplifiers, filters, AGC circuits as required), a modem 2603 having QPSK continuous modulation for downstream transmission with RS FEC, scrambling and sync as described above in conjunction with the ds.block, and a burst modem with TCM and RS decoding and the ability to detect the various upstream primitives 30 described above, a MAC Controller 2604 as described in conjunction with Figure

25, and a Control Unit 2605, based on a microprocessor circuit and connected via data or I/O buses to all other subsystems (connection not shown in Figure 26). An interworking Function 2606 converts the ATM cells to and from the MAC Controller 2604 to whatever format the carrier network requires, such as ATM, 5 Frame Relay or narrow Band ISDN. This function is thus application specific and, in most cases, can be found in existing ATM switches and multiplexers. A line interface 2607 converts the traffic of the Interworking Function 2606 to the network format such as T3/E3 interfaces. As an option for improving cellular network coverage by minimizing interference from geographically adjacent cells, 10 an Adaptive Radio-resource Manager (ARM) Controller 2608 may be included. The ARM Controller is a microprocessor application that responds to commands from a network management system application that coordinates frequency/time activities among multiple sectors and cells. For example, if the network management system finds that a particular ST interferes with another base station, 15 the network management system may instruct that base station to skip those cell slots affected or shift the ST entirely to another frequency. The ARM controller 2608 makes the Base Station Controller capable of receiving such commands from an external controller. The key element for ARM operation is global synchronization of all sectors and cells, as described above. By having all base 20 stations maintain a fixed relationship of the MAC frame/multiframe bits to the global time reference, it is possible to devise algorithms to map transmission from an ST in one sector to interference in another sector or cell. Thus the timing generator 2501, shown in Figure 25, is locked to global time and, in effect, acts as a real time clock. It should be clarified that all real time clocks need not be in 25 identical phase in each cell, as long as they maintain the same difference with each other for a long time. Multiple channels are processed by repeating the same channel structure 2609 as many times as needed. These channel controllers may need to share or switch data among themselves, which can be accomplished via a bus 2610. Finally, all controllers can share the same enclosure or equipment rack 30 to form a base station. Each Base Sector Controller has a coax cable leading to a

Base Radio Unit (BRU) 2611. The BRU includes IF circuits, converters, frequency synthesizer, amplifiers and a diplexer, driving the sector antenna via a waveguide. Such BRUs are commercially available. For example, Netro Corporation of Santa Clara California has a BRU for 38 GHz which, with proper 5 scaling, can be redesigned for other frequencies.

The sector antenna is a pyramidal horn with a rectangular aperture and optional modifications as described below. To minimize interference and to maximize frequency reuse, special care is taken of the Base Antenna. As seen in Figure 27, one potential mode of interference is a subscriber terminal 2700 10 receiving from Base Station A with radiation pattern 1, which also receives from base station B with radiation pattern 2. If pattern 2 is in a different frequency than 1, interference is negligible. It is assumed here that base stations located further away, say another cell diameter behind B, are too far to cause significant interference. In this simple scheme, two frequencies are sufficient to avoid 15 interference. In fact, when multiple cells are drawn together, as shown in Figure 30, two frequencies are sufficient to avoid the interference mode of patterns 2 to 1 in Figure 27. Figure 30 is a lattice based on a four cell structure 3000. This structure has one drawback: some of its sectors are wider than the others. If this is not acceptable, a three-frequency symmetrical solution also exists, as shown Figure 20 31.

The Antenna needs to have a wide pattern in the horizontal dimension, such as 30, 60 or 90 degrees. In the vertical dimensions it may stay narrow, say a 12 degrees beam width, allowing it to improve the gain. However, nearby STs may fall into zeros in the radiation pattern, as shown in Figure 28. This is avoided by 25 allowing a small phase deviation in the horn aperture. A quarter wavelength seems a good compromise between main lobe beam spread and side lobes flattening. This reduction is accomplished by a choice of horn geometry or by intentional aberration in a dielectrical lens. A complete antenna is shown in Figure 29. Its dimensions are about 10 to 20 cm in the longest direction, thus it is fairly small. 30 The pyramidal horn 2900 may include a lens 2901 of near cylindrical shape and

absorbing walls 2902, for adjusting beam width and allowing said radiation pattern to roll off in the horizontal dimension to avoid interference from a pattern 3 to ST 2700 shown in Figure 27.

CLAIMS

1. A wireless metropolitan area network including:
 - at least one base station having a plurality of sector antennas and a MAC controller, said station transmitting and receiving by means of said sector antennas;
 - 5 a plurality of subscriber terminals (STs) located within a sector area, each ST including
 - a directional antenna,
 - a MAC processor, and
 - 10 circuitry for requesting bandwidth through a plurality of contention slots, said circuitry receiving transmission grants from said MAC controller and transmitting ATM cells including a MAC overhead to said base station.
- 15 2. The network of Claim 1, wherein said MAC controller includes support for at least three types of grants.
3. The network of Claim 1, wherein said MAC controller includes support for ATM cell slot, contention slot and admission slot grants.
- 20 4. The network of Claim 2, further including bitmap slots.
5. The network of Claim 1, wherein said STs receive only one grant per slot and transmit on one of said slots a fixed time interval after receiving said grant.
- 25 6. A method for error correction encoding of blocks, each block consisting of a single ATM cell having a MAC overhead and at least one symbol, including the steps of:
 - (a) encoding each of said blocks with error correction bits comprising more than 10% of the size of said block; and

*

(b) trellis code modulating each of said blocks with a trellis code based on a constellation of M bits per each symbol of said block, so that a resulting code rate is higher than $(M-1)/M$.

5 7. A subscriber terminal for a metropolitan area network including a radio unit having an enclosure and an attached lens horn antenna.

8. The structure of Claim 7, wherein said horn structure is an integral part of said enclosure.

10 9. The structure of Claim 8, further including a microprocessor having built-in ATM formatting capabilities.

10. A method of for transmitting constant bit rate ATM cells over a point-to-
15 multipoint network including the steps of:

(a) transmitting a grant to a subscriber terminal within a first fixed time window of the ideal transmission time for a virtual circuit; and

(b) having said grant be used by said virtual circuit that also maintains a second time window only if said time window has not expired.

20 11. The method of Claim 10, wherein during step (b) if more than one virtual circuit exists on a subscriber terminal the grant is used by a virtual circuit with the oldest non-expired window.

25 12. The method of Claim 11, further including the step of transmitting a time stamp with each of said ATM cells that has used said grant, wherein cell delay variation is reduced by adding a compensating delay to said cell upon arrival at the receiving end of said network.

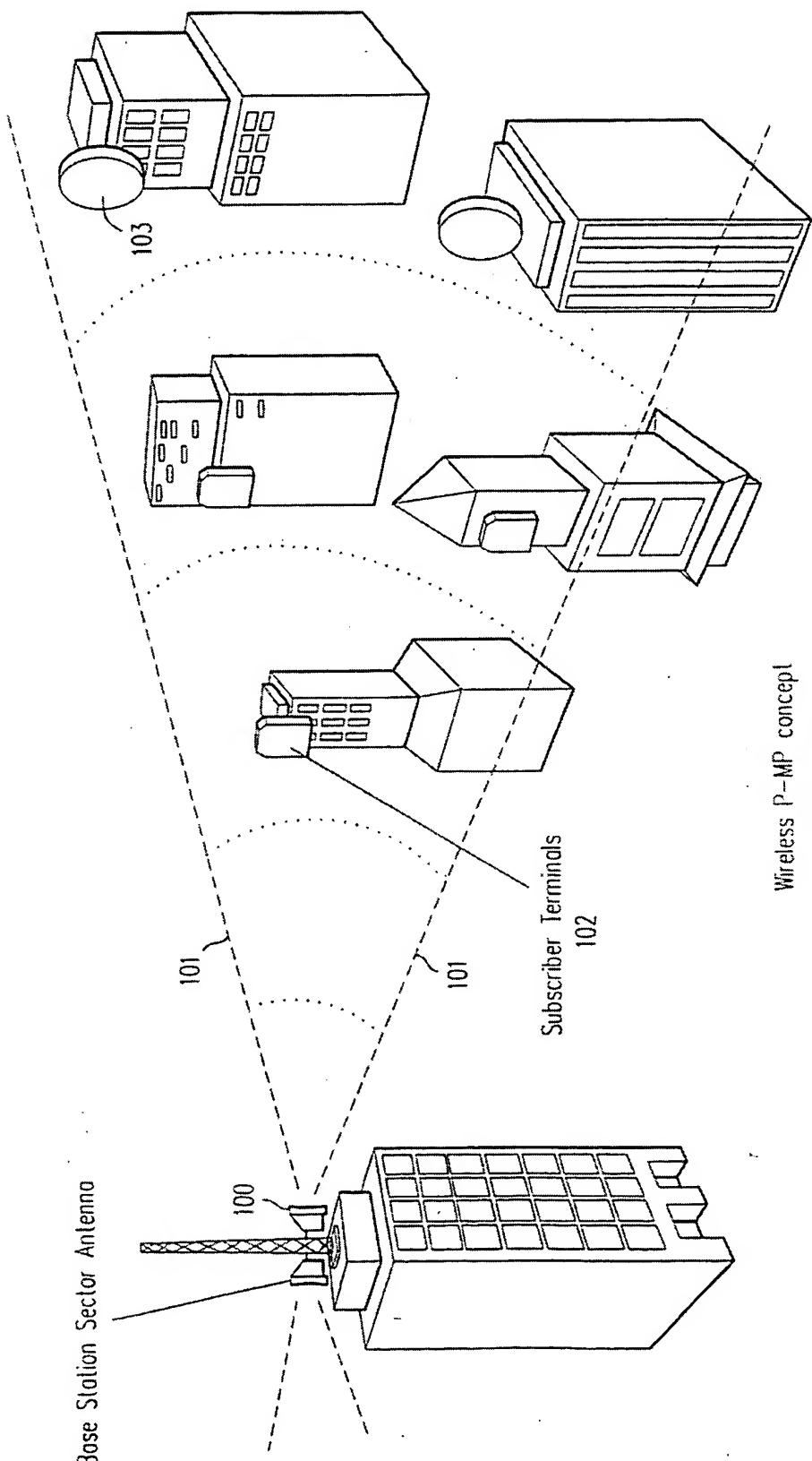


FIG. 1

Wireless P-MP concept

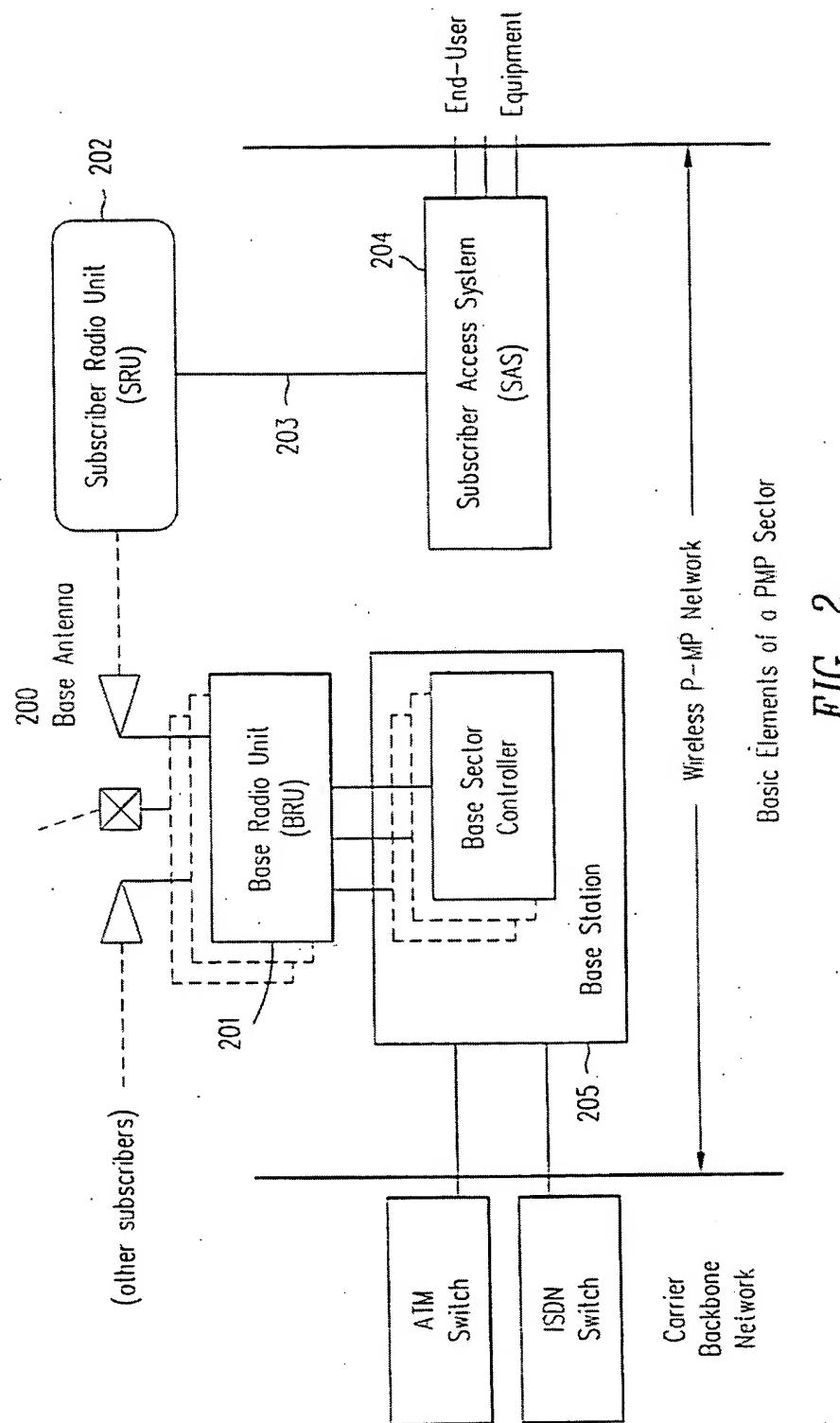
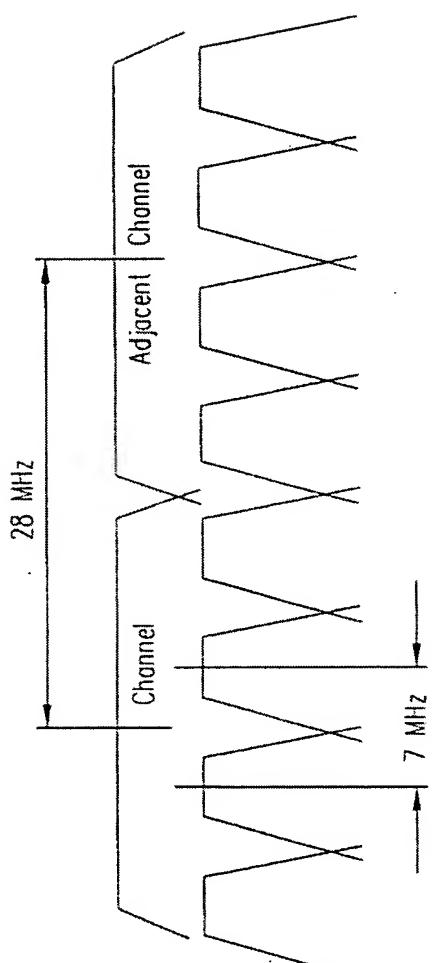
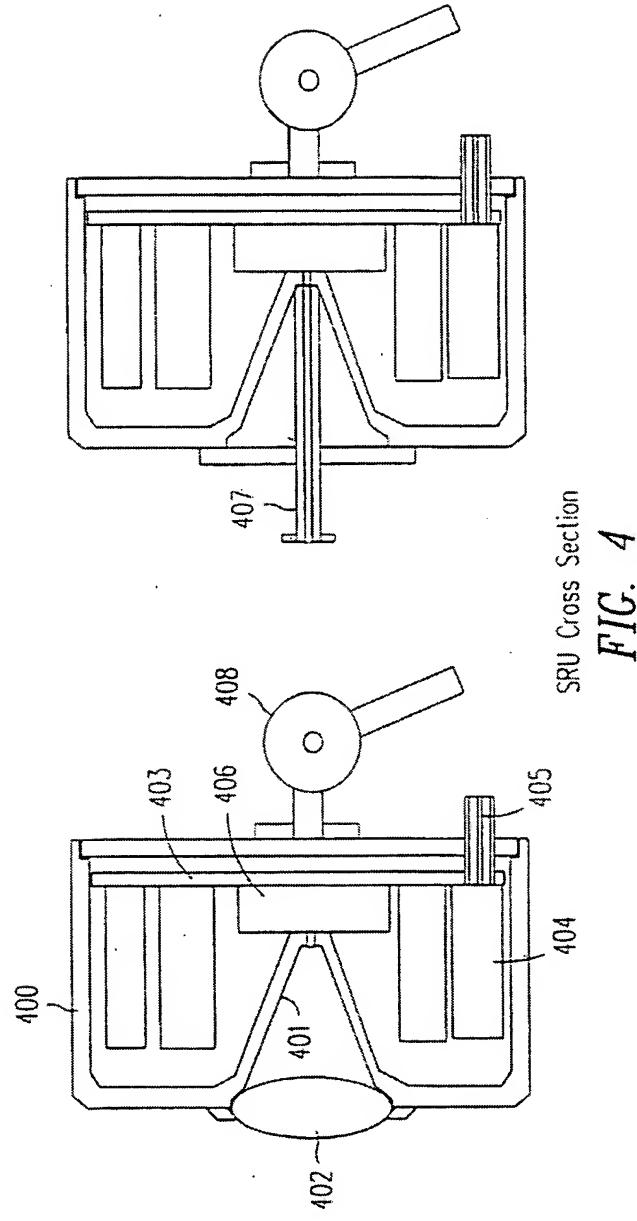


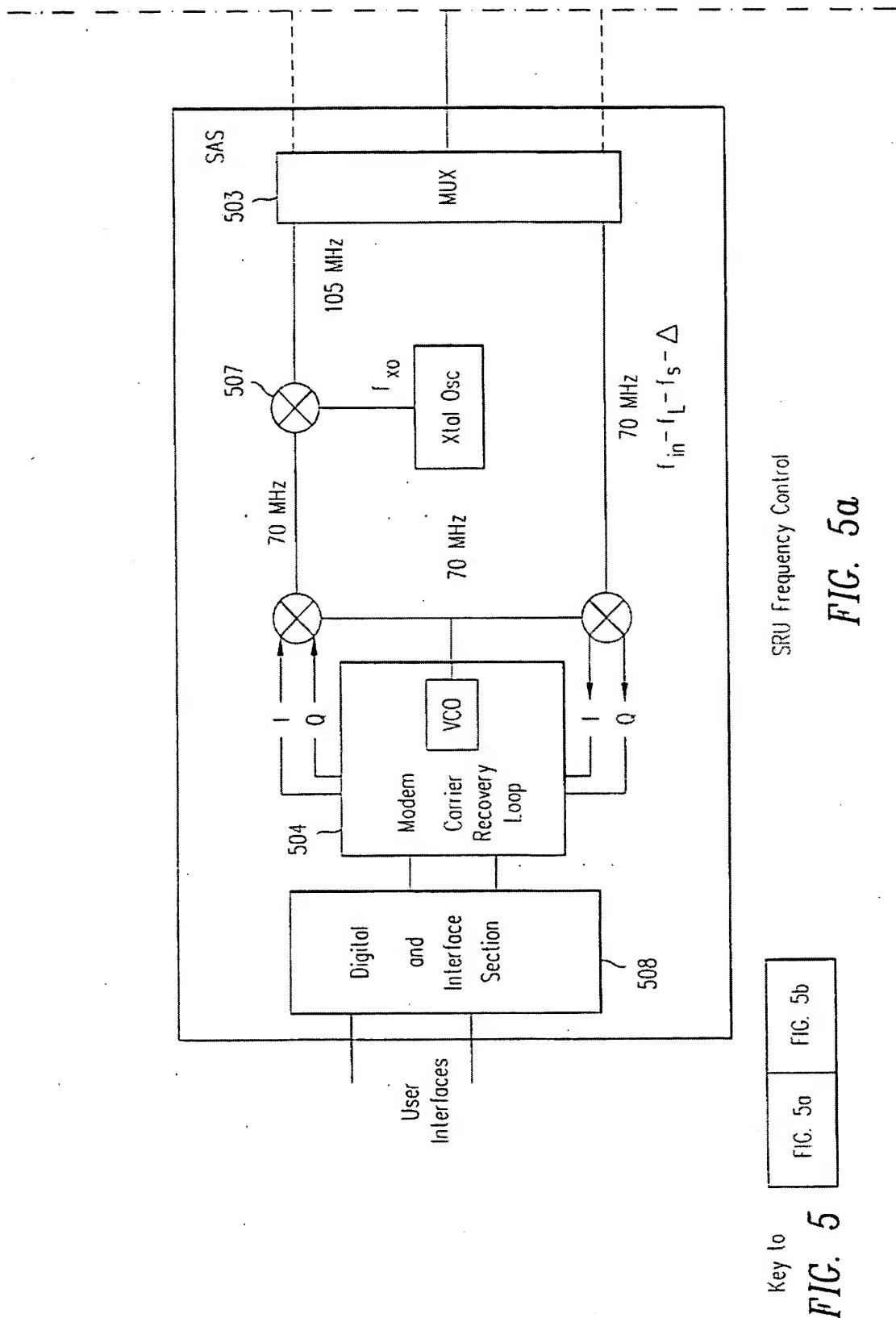
FIG. 2



FDM Structure
FIG. 3



SRU Cross Section
FIG. 4



Key to
FIG.

FIG. 5a

SRU Frequency Control

SUBSTITUTE SHEET (RULE 26)

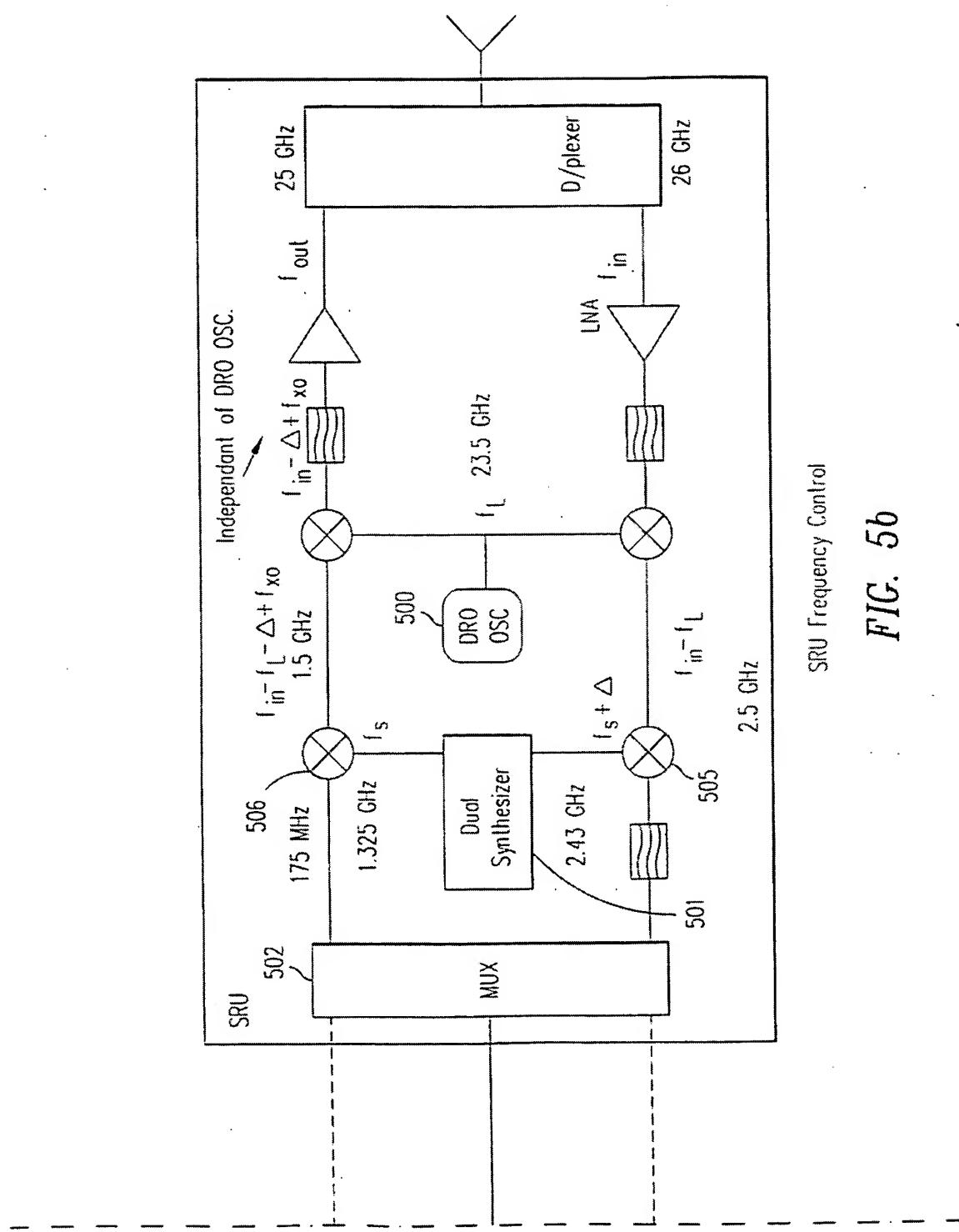
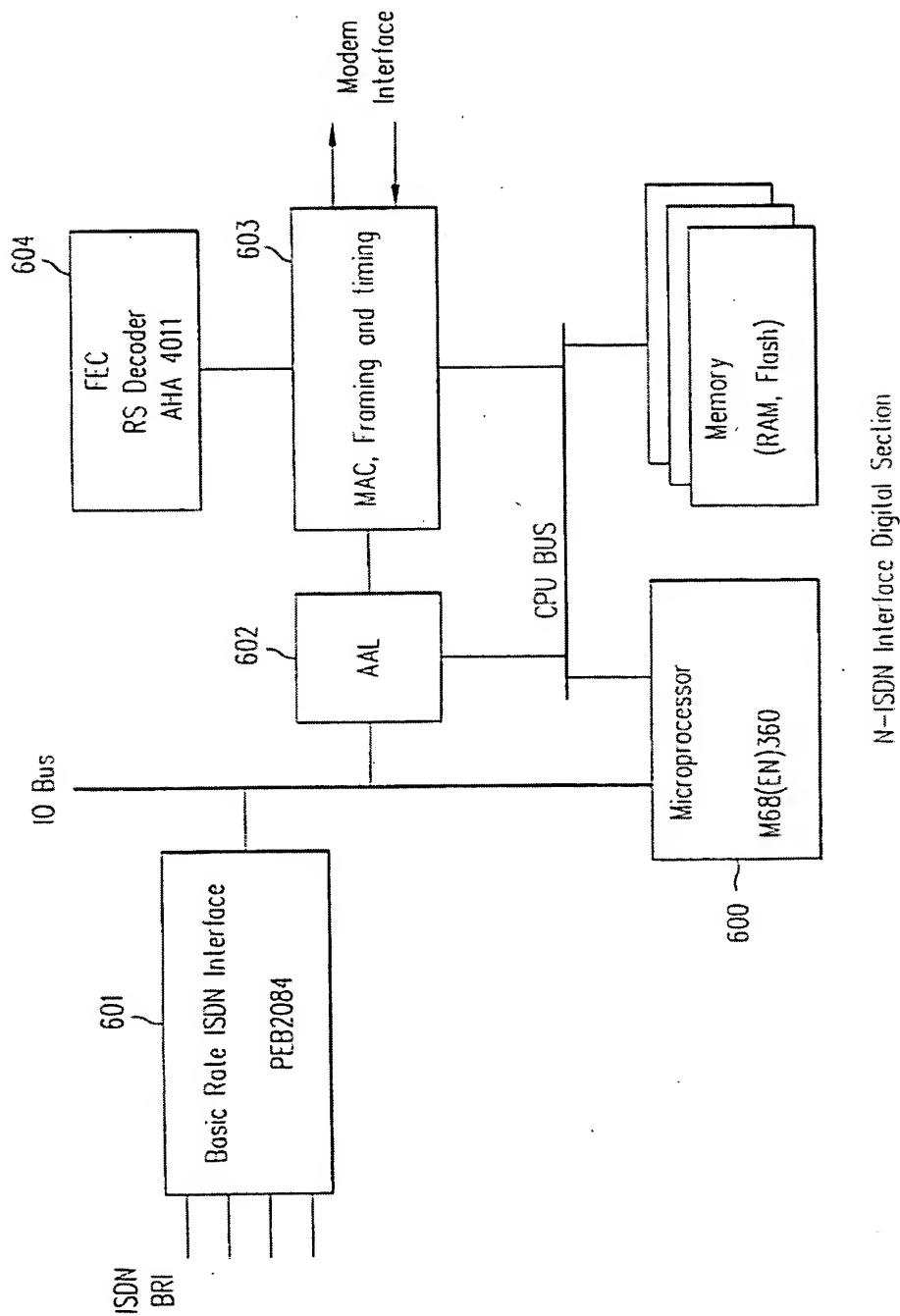


FIG. 5b

SRU Frequency Control

6/22



N-ISDN Interface Digital Section

FIG. 6

7/22

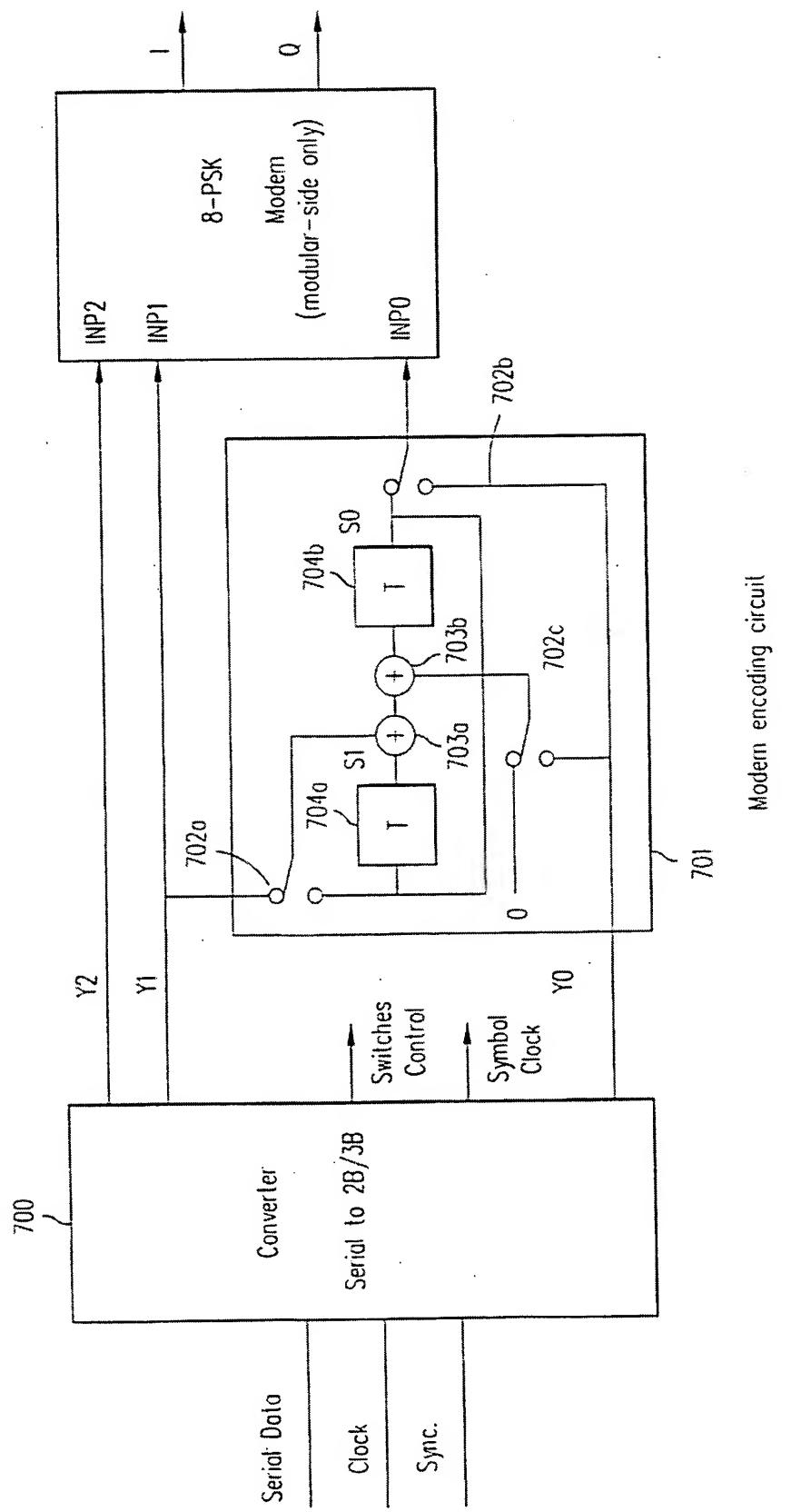


FIG. 7
Modem encoding circuit

8/22

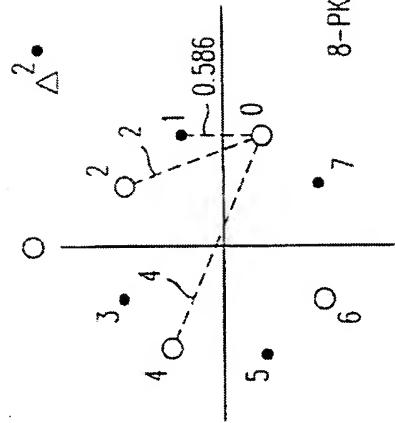


FIG. 8

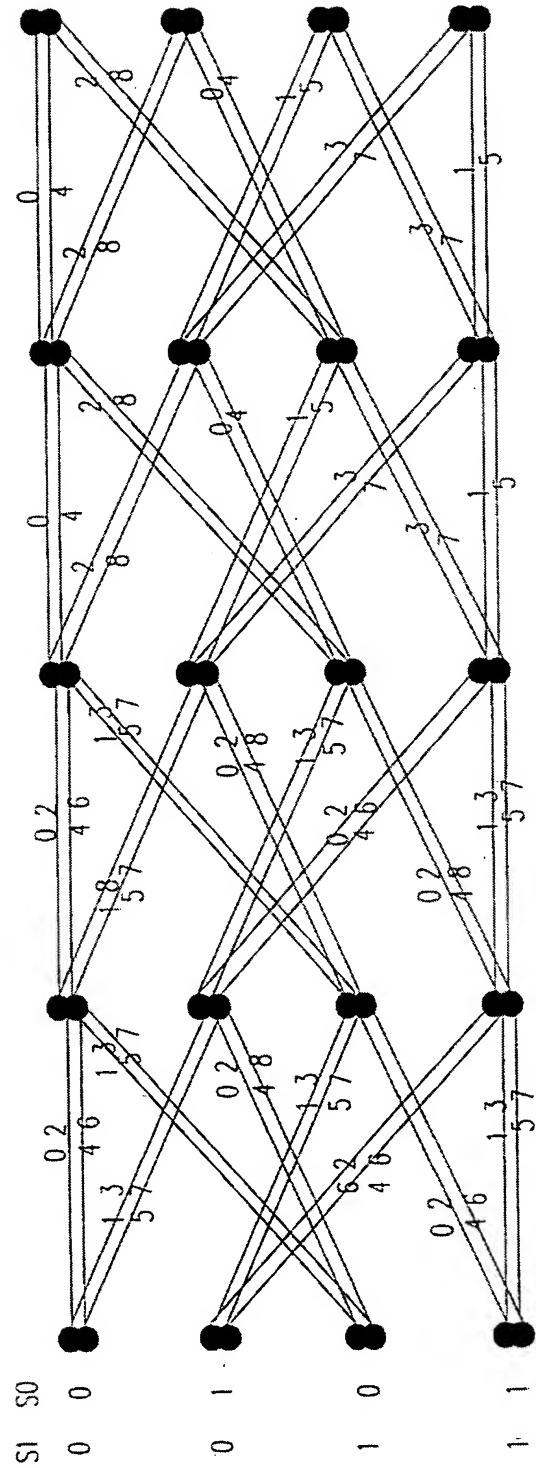
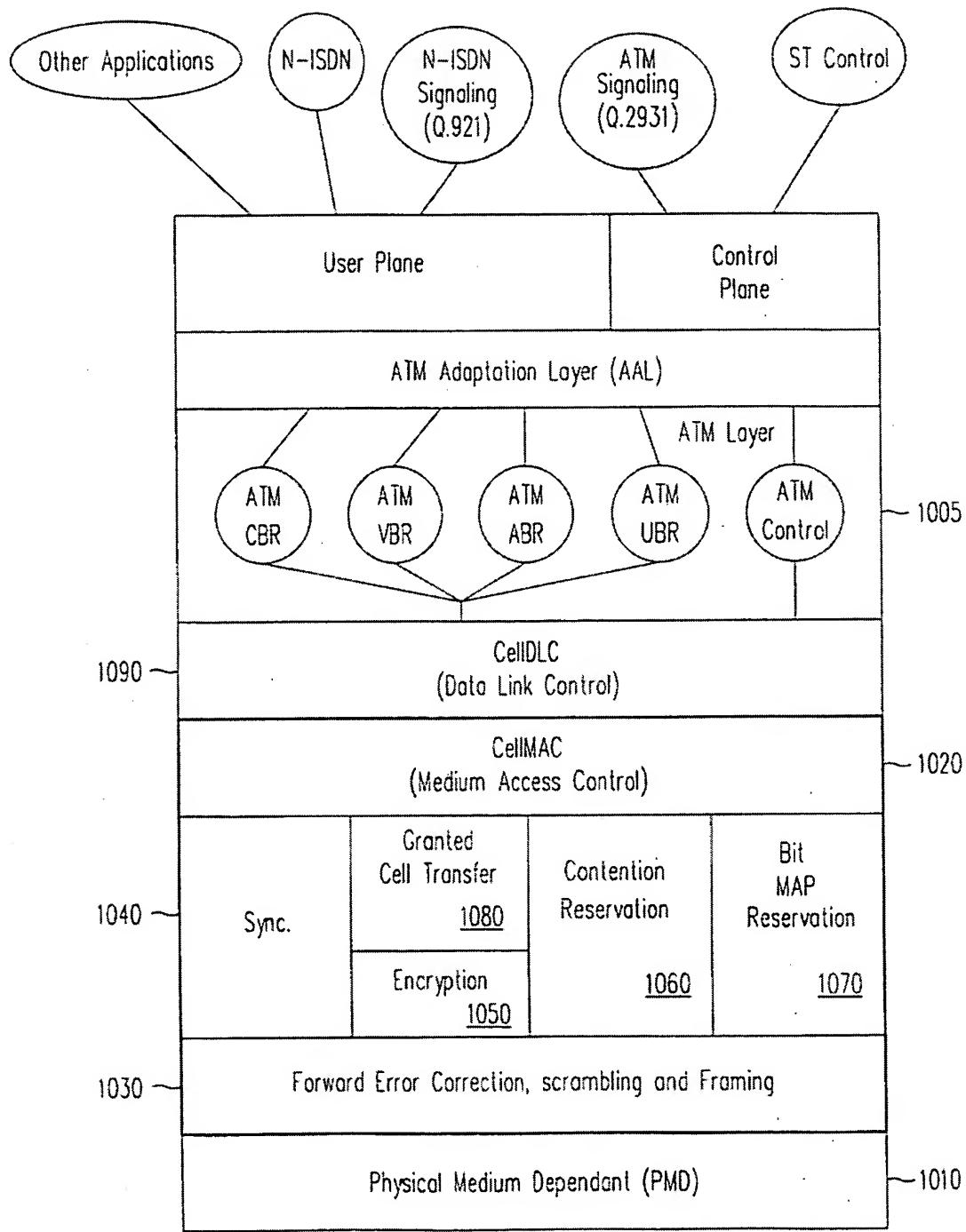


FIG. 9

9/22



Wireless Air Interface Reference Model

FIG. 10

10/22

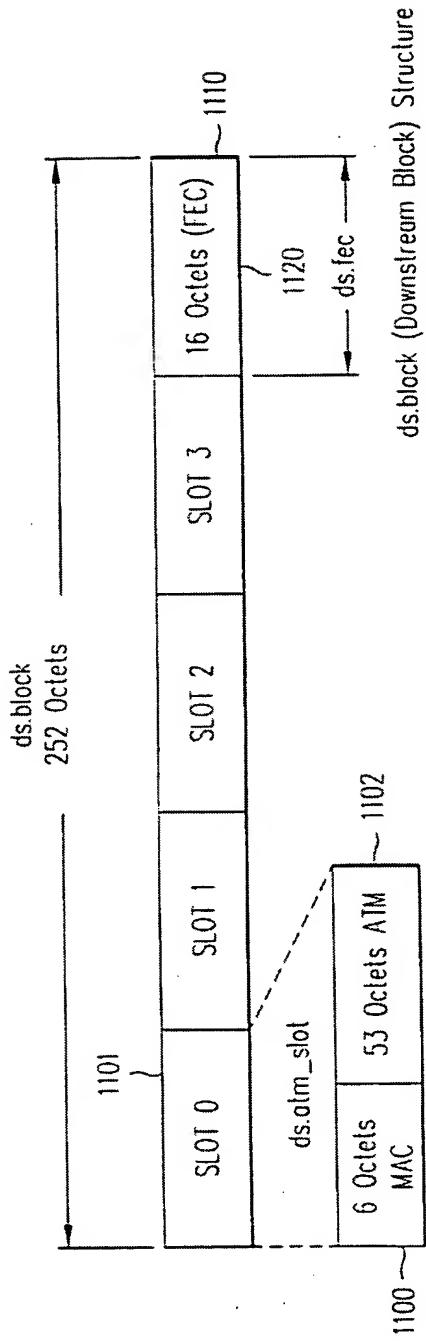


FIG. 11

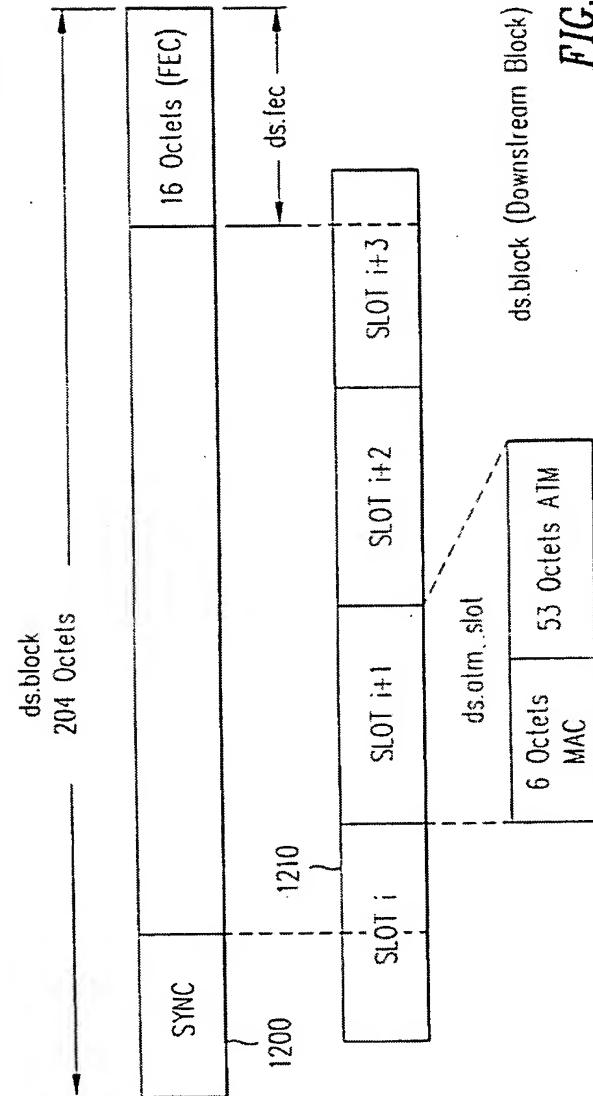


FIG. 12

11/22

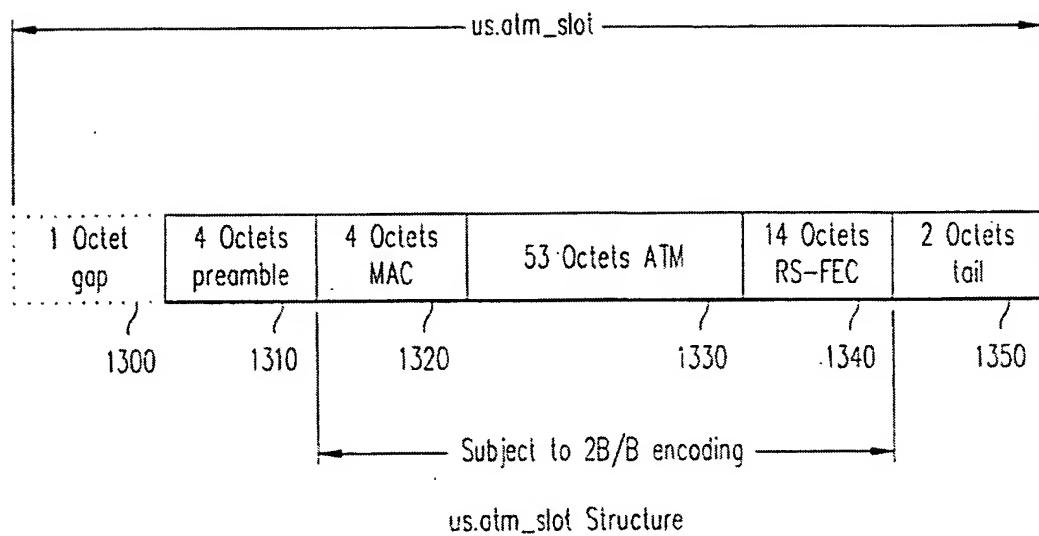


FIG. 13

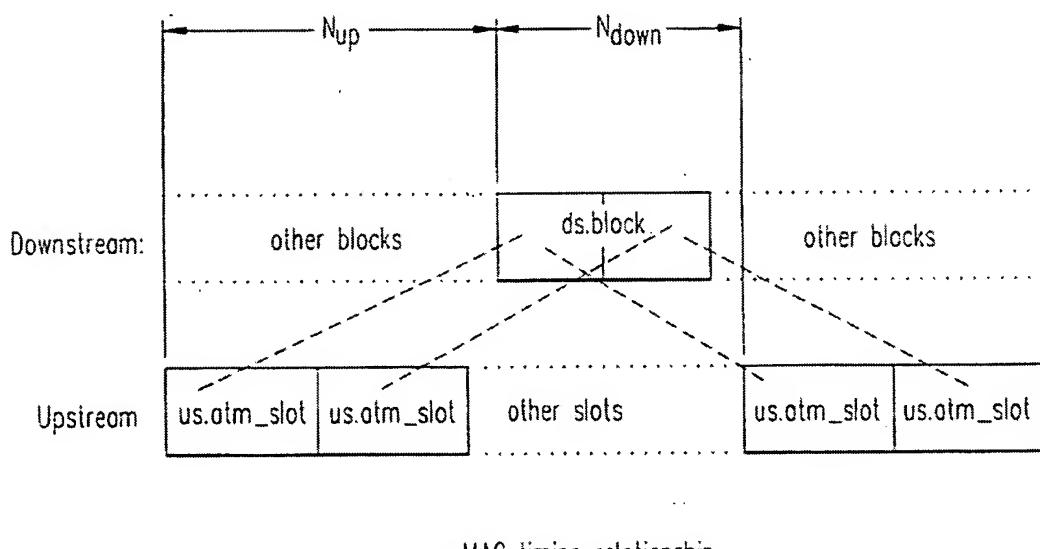
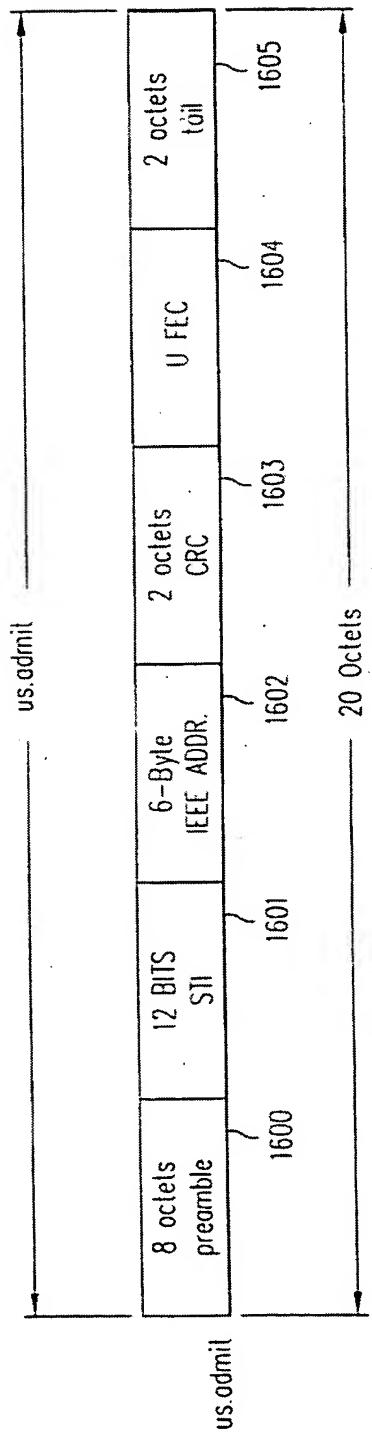
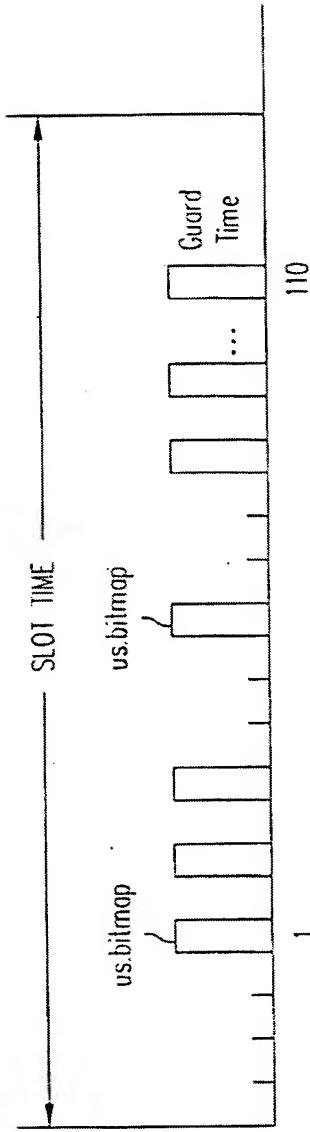


FIG. 14

12/22



Admission request format
FIG. 16



Bitmap Slot Structure
FIG. 15

13/22

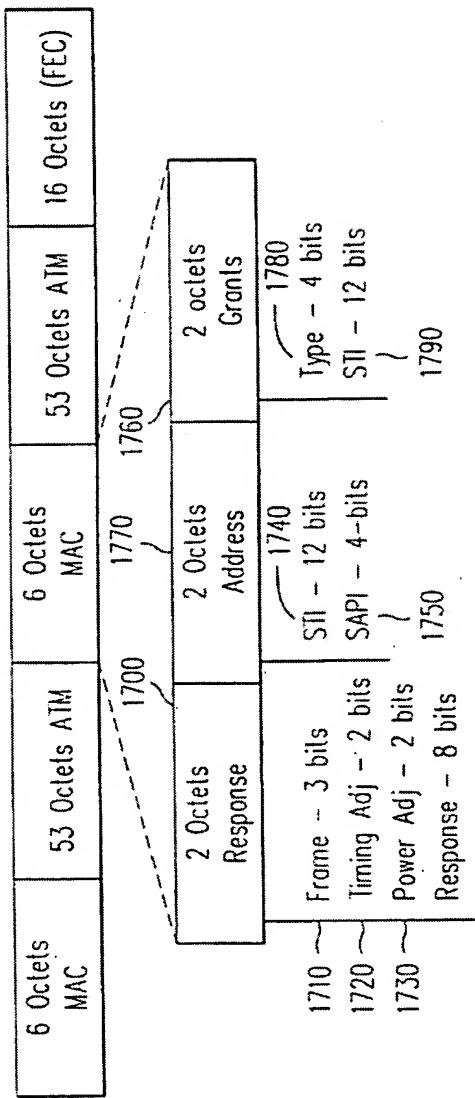


FIG. 17

Downstream CellMAC Overhead Structure

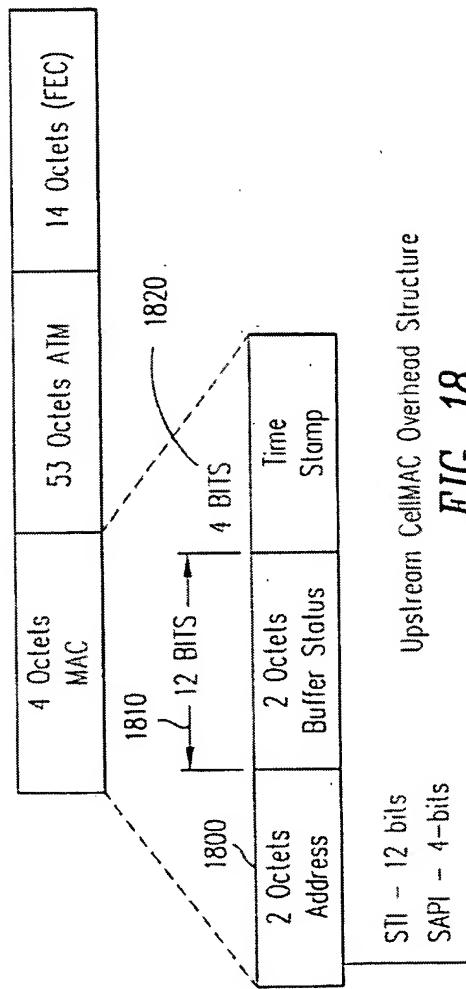
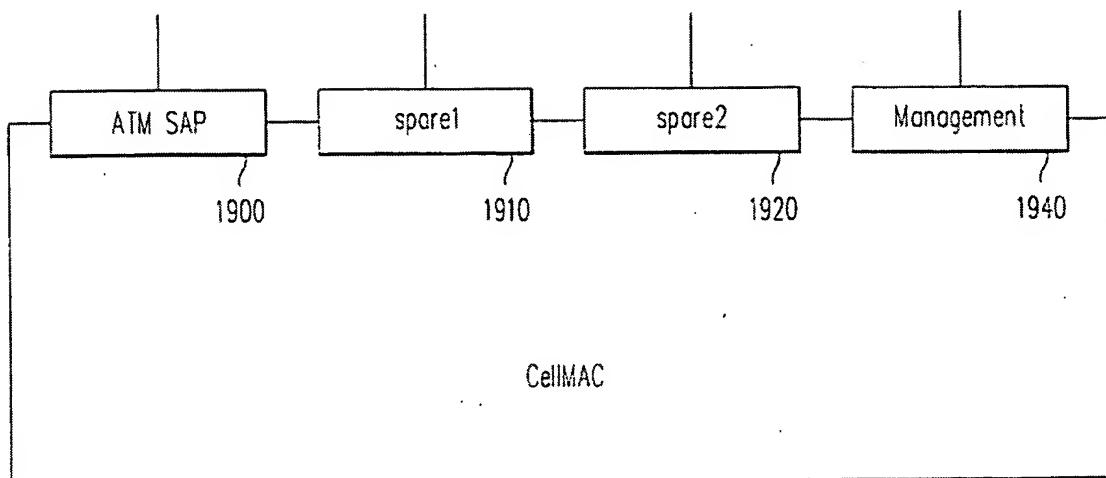


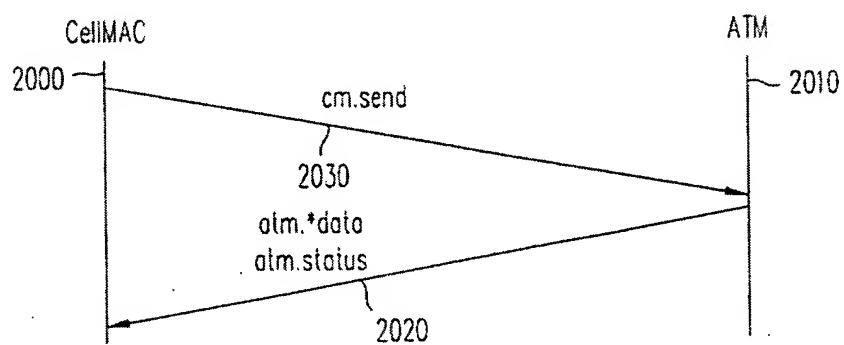
FIG. 18

14/22



The CellMAC SAPs model

FIG. 19



ATM cell transmission requested by CellMAC

FIG. 20

15/22

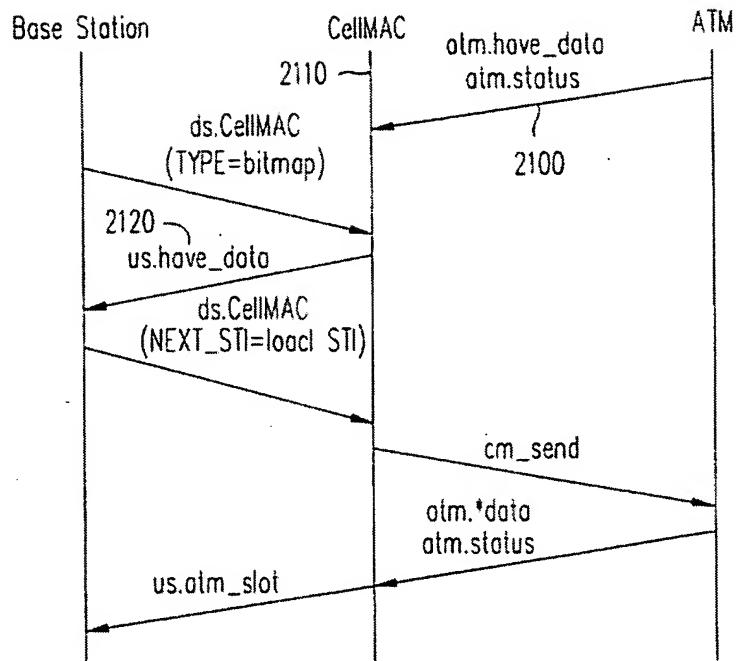


FIG. 21 ATM cell transmission requested by ATM layer - bitmap available

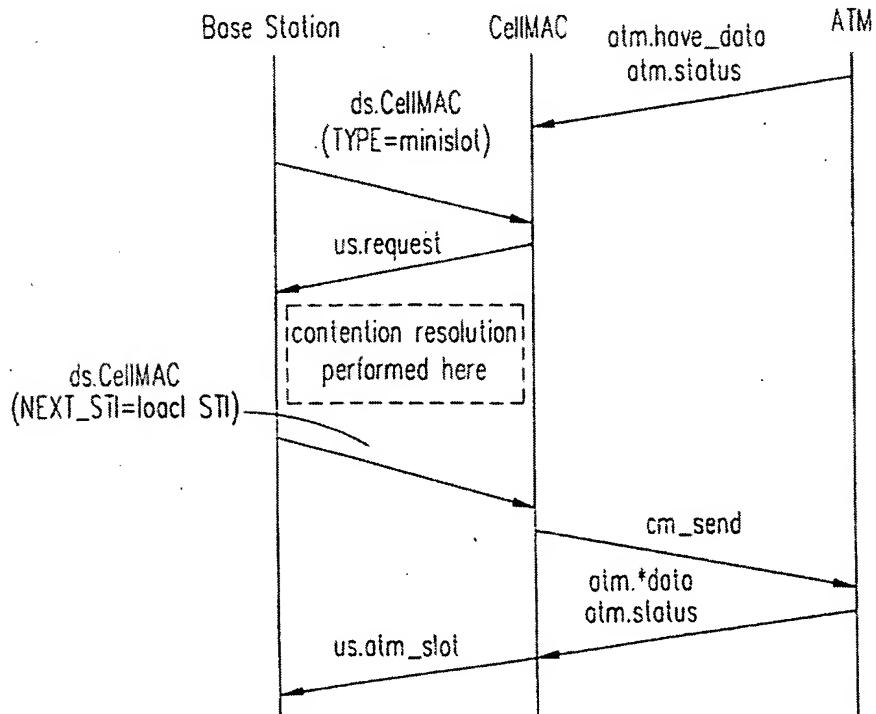


FIG. 22 ATM cell transmission requested by ATM layer by a minislot contention

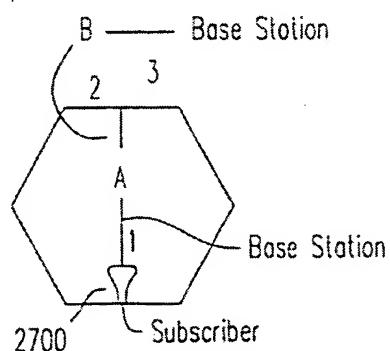
16/22

Slot skipped because
no grant received

us.slot.0			4	8	11		16		
us.slot.1			1	5		12	14		
us.slot.2			2	6	9		15		
us.slot.3			3	7	10	13			

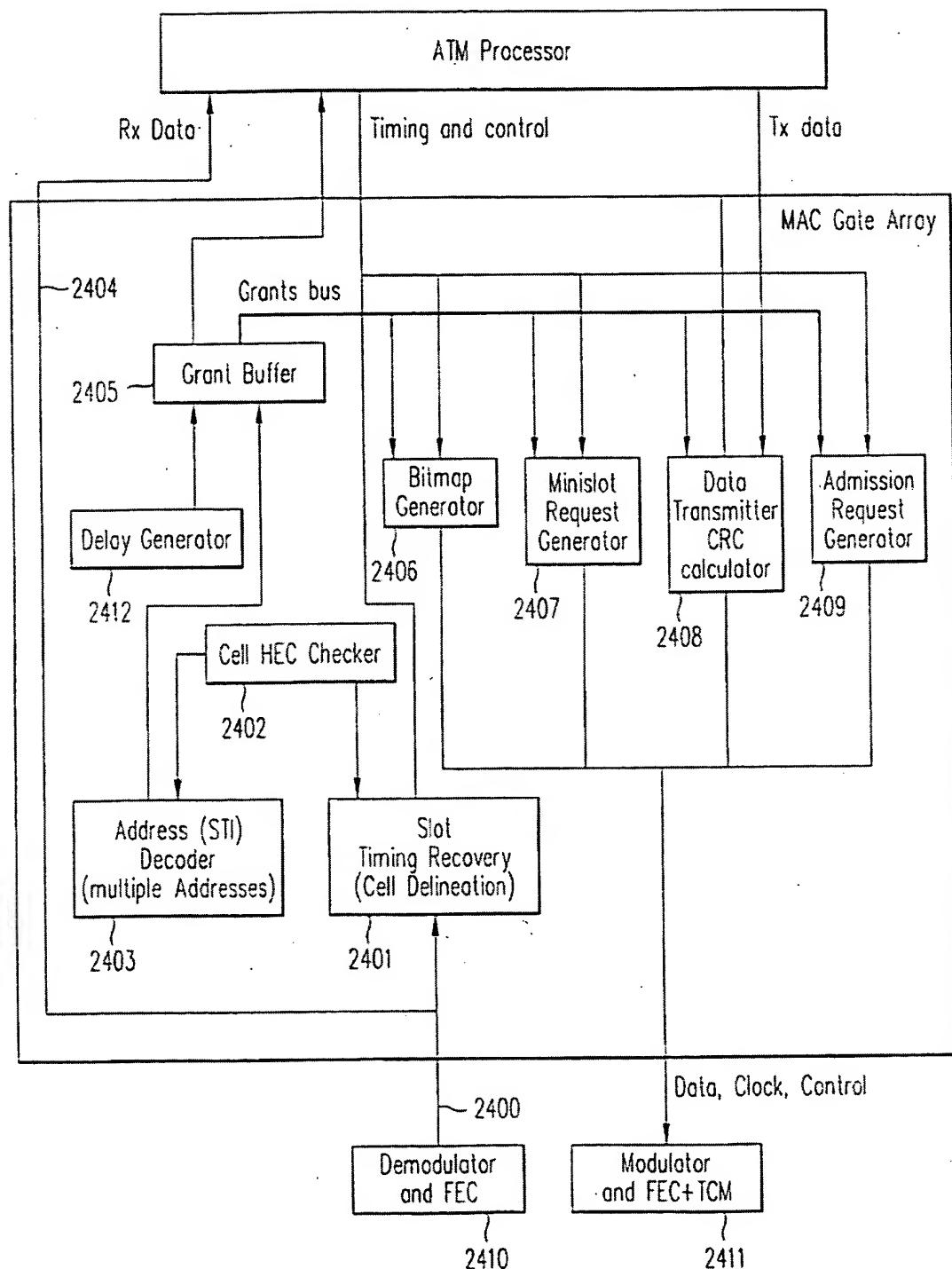
Parallel Cell Transfer

FIG. 23



Roll-off interference

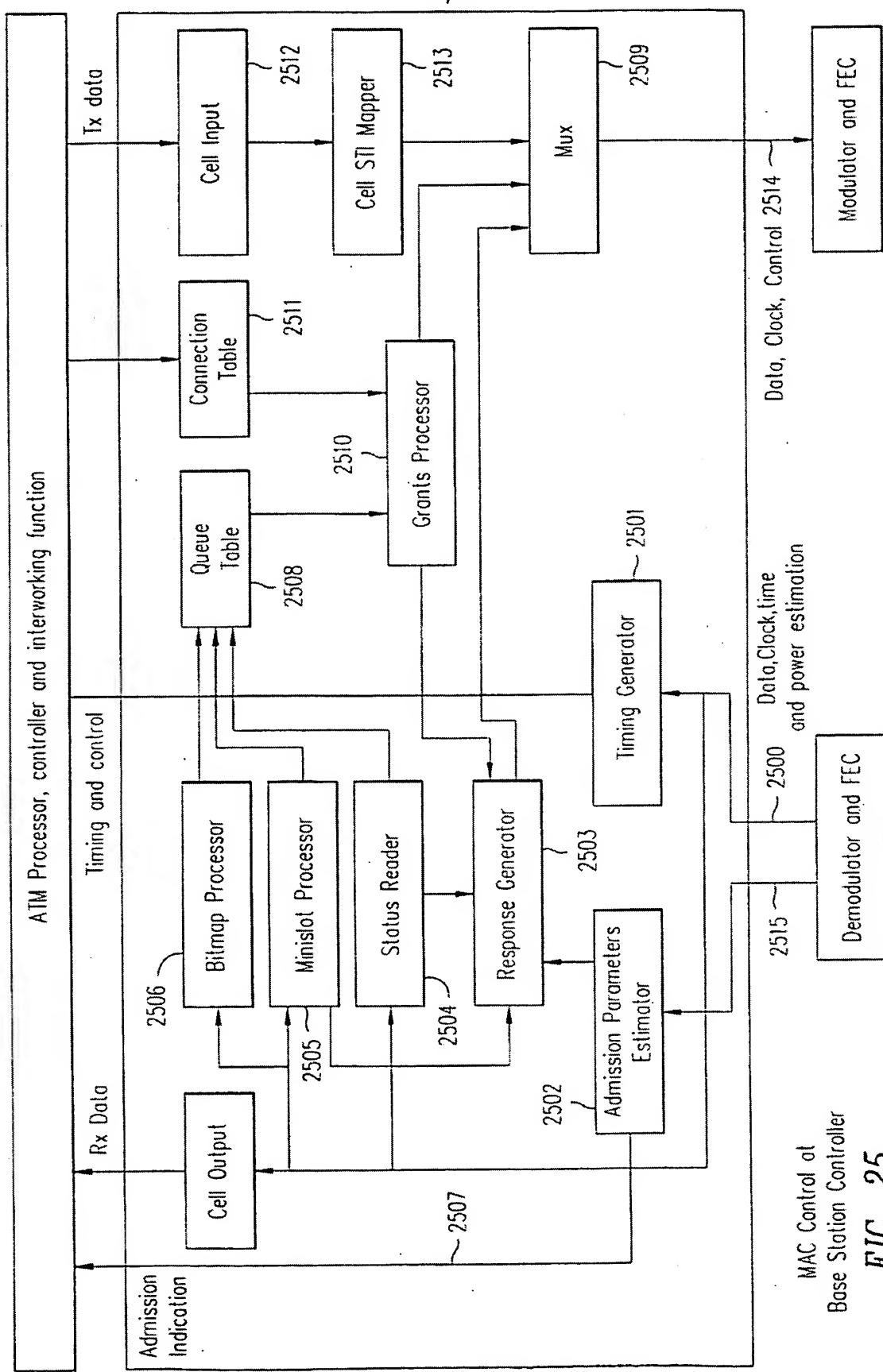
FIG. 27



MAC Gate Array Block Diagram

FIG. 24

18/22



19/22

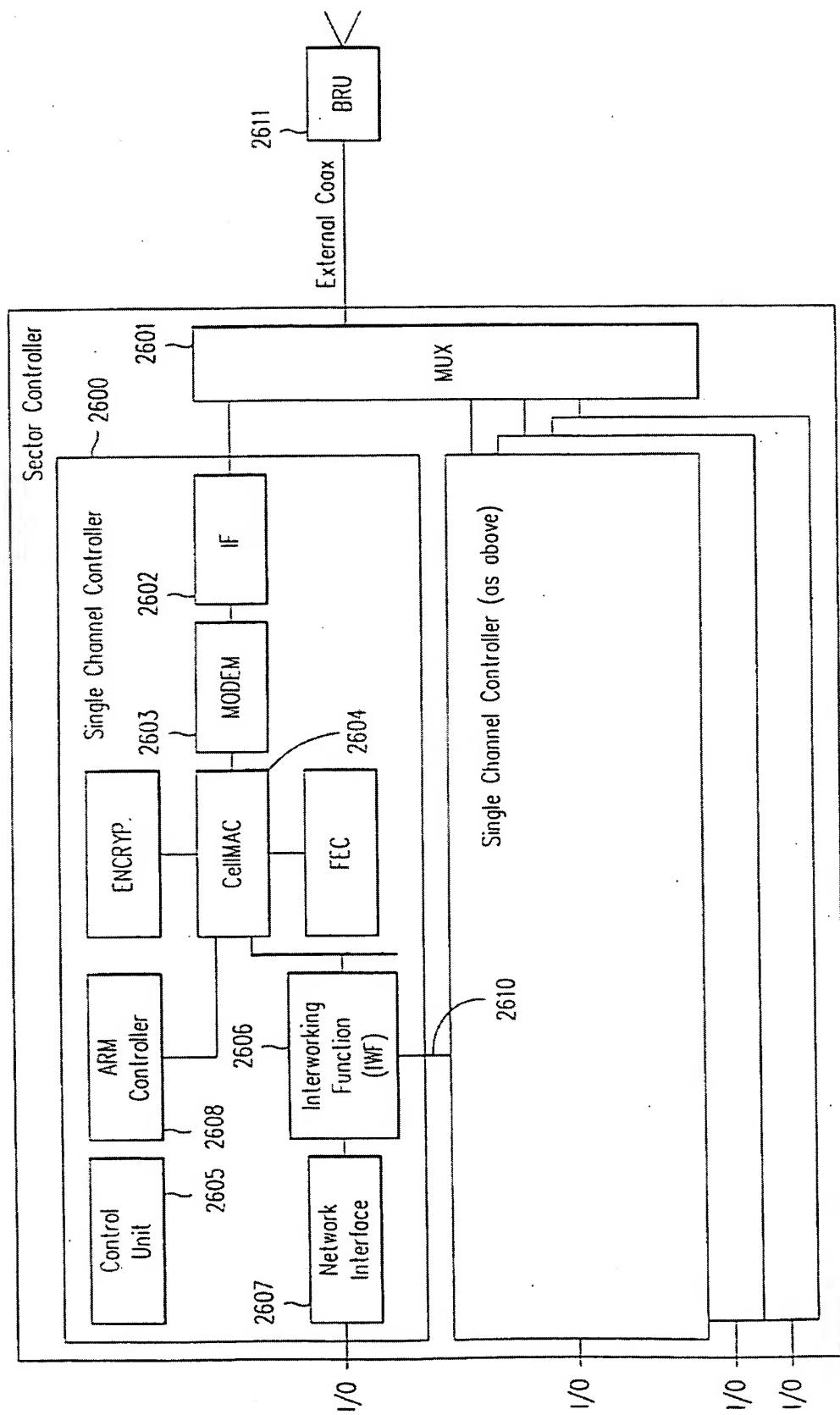


FIG. 26 Base Station Controller Block Diagram

20/22

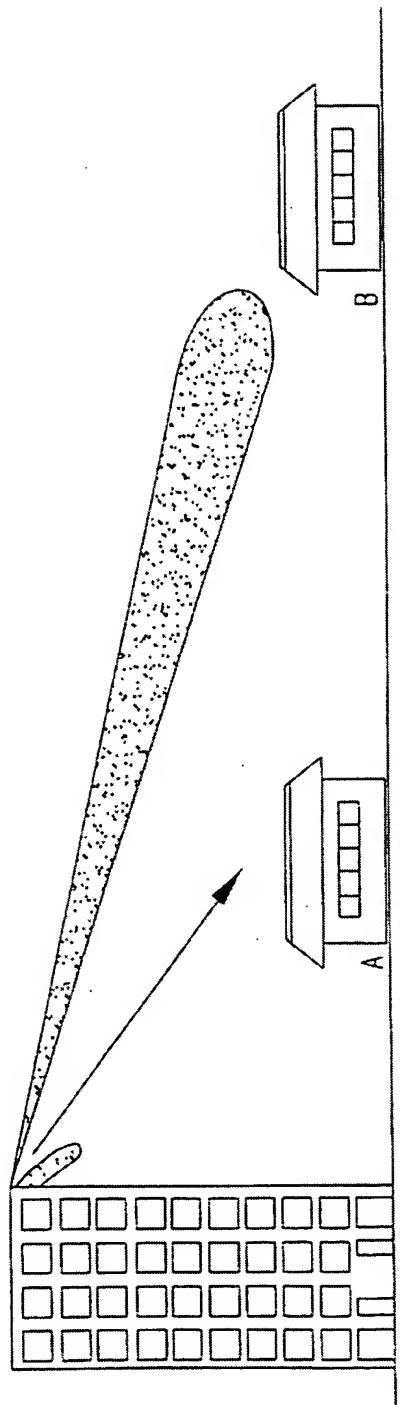
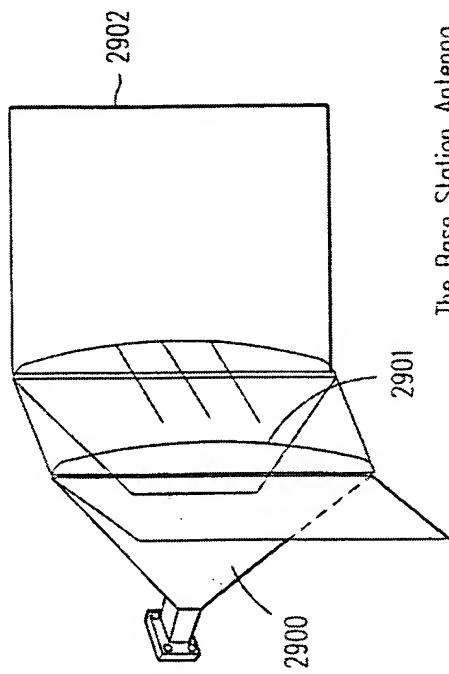
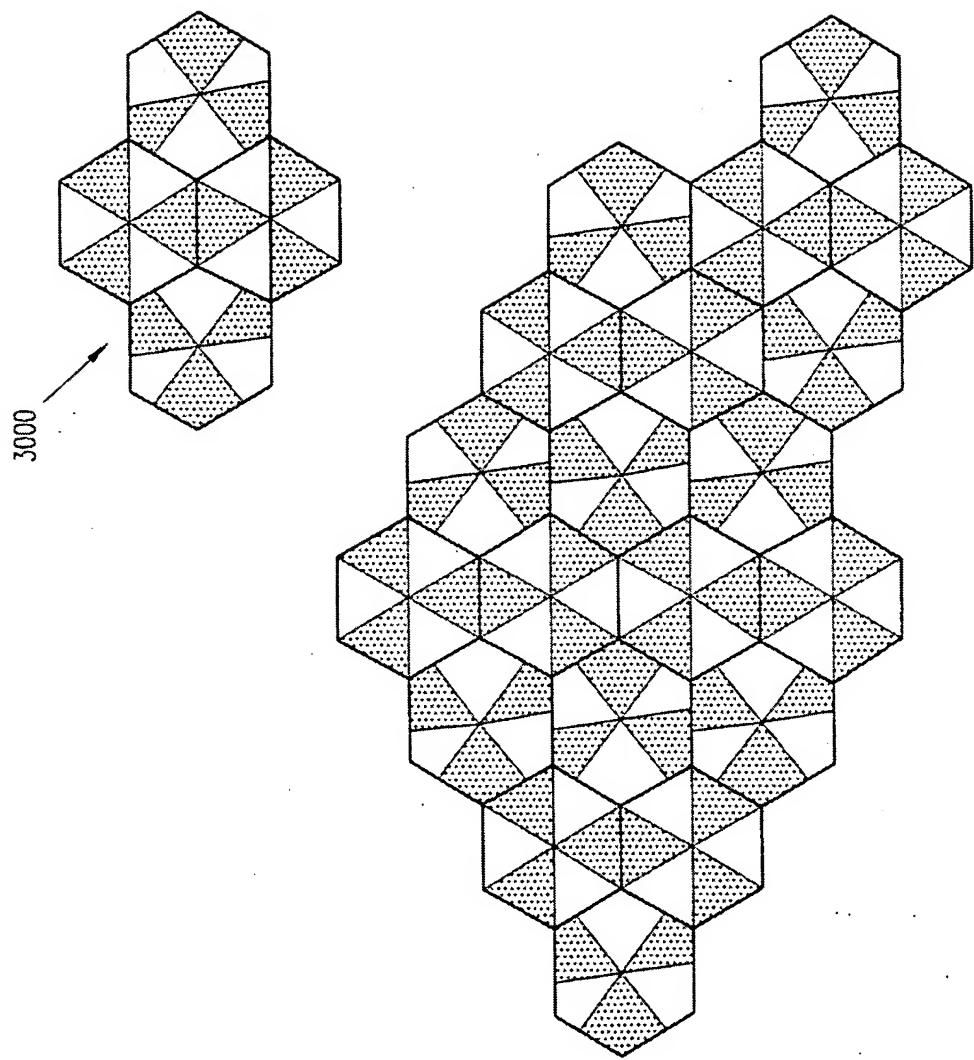


FIG. 28

Vertical radiation pattern effects



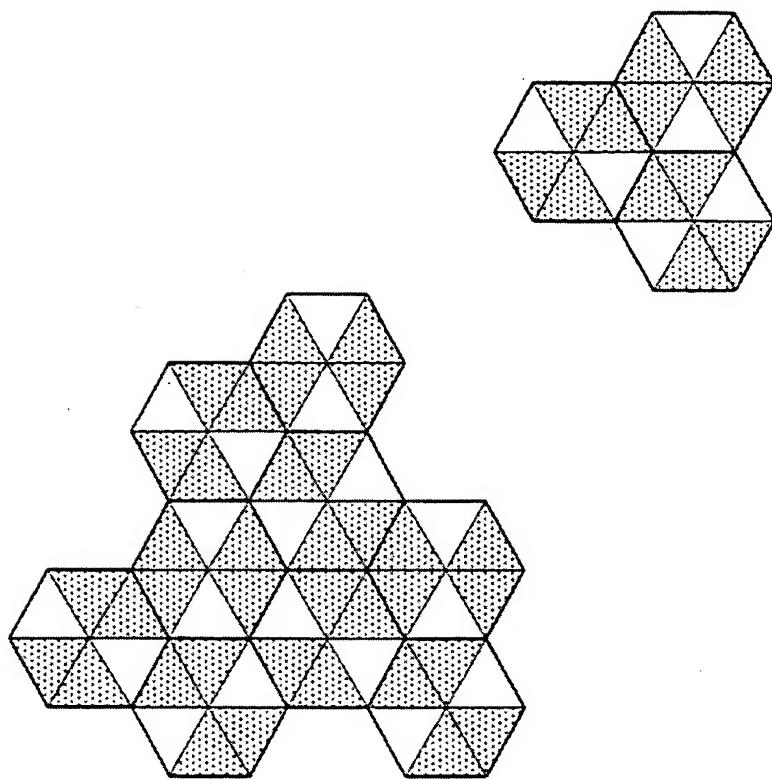
The Base Station Antenna
FIG. 29



Coverage Map with one pair of frequencies

FIG. 30

22/22



Symmetrical cellular arrangement with three transmitting channels

FIG. 31

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US97/15119

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04L 25/56; H04Q 7/24

US CL :370/328, 337, 347, 348, 349, 395

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/328, 337, 347, 348, 349, 395

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, IEEE on disc

search terms: wireless, atm

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,426,442 A (HAAS) 20 June 1995, column 1, lines 35-40 and column 3, lines 23-28.	7, 8
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Y		9
Y	US 5,490,144 A (TRAN ET AL) 06 February 1996, column 2, lines 33-36.	4
Y	TSLE, K.Y. ET AL, Performance Comparison of High Level Modulation Techniques For Land Mobile Communications, IEE Colloquium on Advanced Modulation and Channel Coding Techniques for Mobile and Personal Communications, Digest No. 206, November 1992, pages 3/1-3/6, especially page 3/2.	6

Further documents are listed in the continuation of Box C. See patent family annex.

Special categories of cited documents:	*T*	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A		document defining the general state of the art which is not considered to be of particular relevance
B	*X*	earlier document published on or after the international filing date
L		document which may throw doubt on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
O	*Y*	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
P	*Z*	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 OCTOBER 1997	23 DEC 1997

Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer  MELVIN MARCELO Telephone No. (703) 305-3900
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INTERNATIONAL SEARCH REPORT

International application No. PCT/US97/15119

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	LAU, R.C. ET AL, Synchronous Techniques for Timing Recovery in BISDN, GLOBECOM '92, IEEE Global Telecommunications Conference, December 1992, Vol. 2, pages 814-820, especially page 816.	12
Y	XIE, H. ET AL, Data Link Control Protocols for Wireless ATM Access Channels, 1995 Fourth IEEE International Conference on Universal Personal Communications, November 1995, pages 753-757.	1-6 and 10-12
Y	HORNEFFER, M. ET AL, Directed Antennas in the Mobile Broadband System, Proceedings IEEE INFOCOM '96, March 1996, Vol. 2, pages 704-712.	1-5
Y	FALCONER, D., A System Architecture for Broadband Millimeter-Wave Access to an ATM LAN, IEEE Personal Communications, August 1996, Vol. 3, Iss. 4, pages 36-41.	9